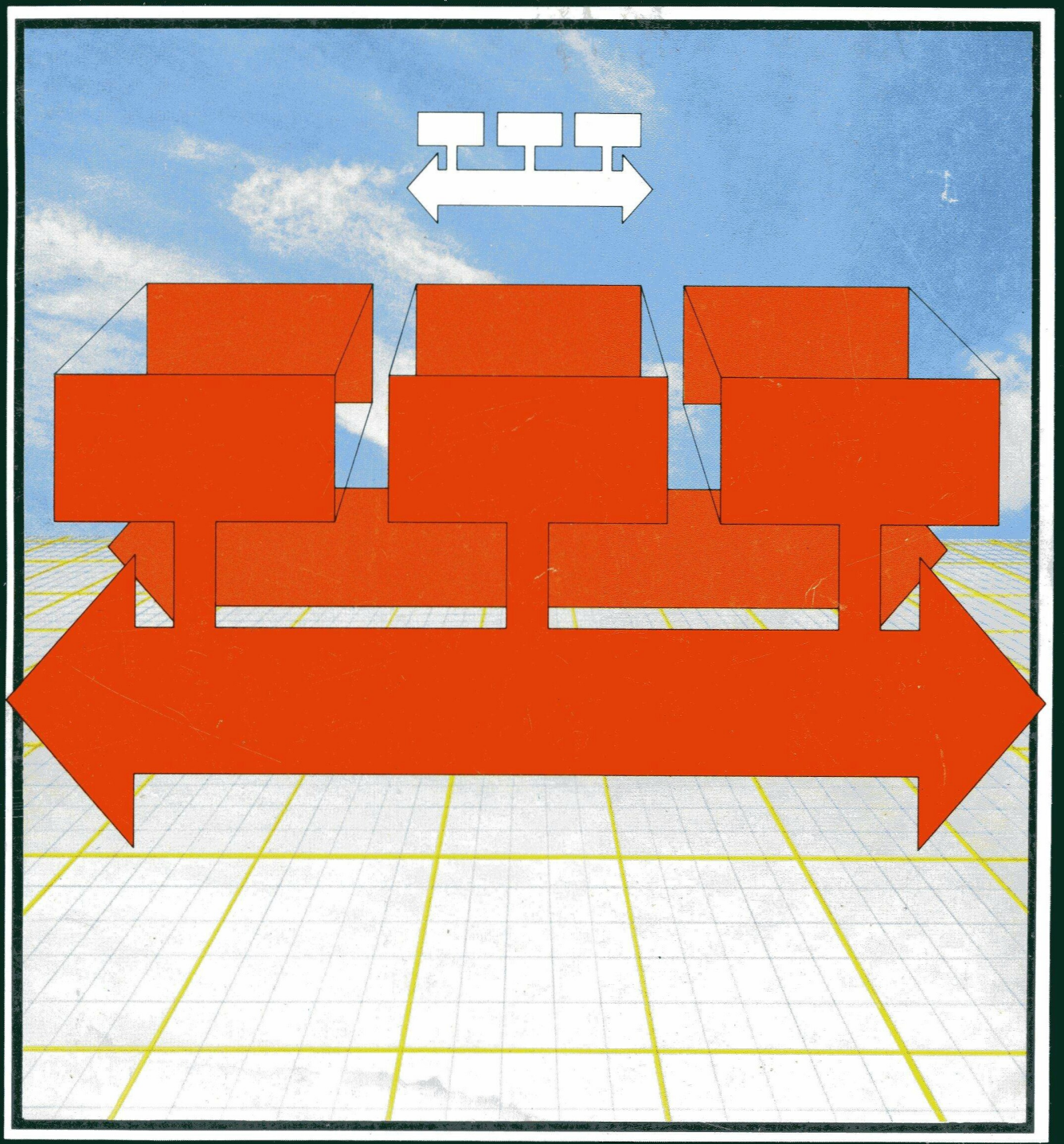
E-BUS SYSTEM DESIGN



TEXAS INSTRUMENTS

E - B U S

S Y S T E M D E S I G N

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September 1981

MP402

8. Other comments concerning E-Bus or standard E-Bus modules from TI: _____

_____

_____

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CONTENTS

E-BUS SYSTEM DESIGN HANDBOOK

This handbook describes the design and method of operation of the E-BUS. Numerous notes and examples are given which are intended to aid the user in the development of his own modules. The handbook serves also as a design aid for the use of the TM990/E Series Microcomputer Modules from Texas Instruments.

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2. E-BUS DESCRIPTION

3. MULTI-MICROCOMPUTER SYSTEMS

4. MEMORY EXPANSION

5. CRU INTERFACE

6. INTERRUPT OPERATION

7. CIRCUIT EXAMPLES

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SECTION 1

INTRODUCTION

The continually increasing degree of integration of semiconductor circuits enables a complete microcomputer to be realised on a single Eurocard (100mm x 160mm). More complex functions can be implemented on a double Eurocard. Using the standard Eurocard format and the accompanying DIN 41612 connector, the E-BUS introduced by Texas Instruments supports the development of mechanically compact microcomputer systems. The large number of manufacturers and suppliers of such mechanical components as chassis and connectors can be used to advantage in the development of cost effective microcomputer systems.

As a bus system capable of multiprocessor operation, E-BUS offers a very flexible interrupt structure, a variable 8 or 16 bit wide data bus and an address range of up to 1 million bytes, as well as three different input/output formats (DMA, memory mapped I/O, and the bit orientated CRU interface of the 99XXX microprocessors).

Current parallel bus structures require significantly more than 100 lines to provide such capability, and use cost intensive and less reliable edge connectors. The number of lines required can be drastically reduced by the use of a multiplexed address, data and interrupt bus.

The multiplexing of the address and data lines on E-BUS does not impose a speed penalty since data from memory is only available to the microprocessor after a specified access time, and on the E-BUS, the changeover from the transmission of address to transmission of data occurs during this time. This handbook also shows that no additional components are required on a memory module for the storing of addresses.

The necessary number of ground and supply lines are also included in the 64 lines which form the E-BUS.

The connectors used are 64 pin units conforming to DIN 41612 (form C, rows A and C used, see also appendix A). Seven pins out of the 64 pin version and the remaining row in the 96 pin option are reserved for later expansion to a 32 bit data/address bus.

1.1 SUPPLEMENTARY DOCUMENTATION

The following Texas Instruments publications were used in compiling this handbook.

1. E-BUS Electrical Specification
2. E-BUS Logical Specification
3. E-BUS Mechanical Specification
4. TMS9980A/TMS9981 Microprocessor Data Manual
5. TMS9900 Microprocessor Data Manual
6. TMS9995 Microprocessor Data Manual
7. 16 Bit Microprocessor Applications Book - Vol.2
8. Applications Report EB135, Transformer Coupled Multi-Microcomputer Interfaces for Industrial Applications
9. Applications Report EB141, Analogue-Digital Converter ADC0808/0816
10. The TTL Data Book (LCC4112)
11. EUROBUG 4 Users Manual - October 1980
12. 9900 Family System Design and Data Book
13. TMS9900 Family Software Development Handbook
14. Component Software Handbook
15. Functional and electrical Specification of Power Supplies for TM990 and TM990/E Microcomputer Boards
16. The Industrial Systems Protocol Functional Specification (#2250632-9901)

1.2 FORMAT OF THE SYSTEM DESIGN HANDBOOK

The E-BUS System Design Handbook is intended to assist both the experienced and the first time user. The handbook is subdivided as follows:

	Chapter
Description of the E-BUS Signals	2
Multimicrocomputer Systems	3
Memory expansion and	4
parallel input/output	4.5
CRU Interface	5
Interrupt Operation	6
Circuit Examples	7
Mechanical Assembly of E-Systems	8

Following the explanation of the E-BUS signals, there is a detailed description of the development of multi-microcomputer systems, memory expansion, CRU input/output and interrupt operation. Chapter 7 contains detailed circuit examples of different E-BUS modules and assumes a familiarity with E-BUS.

Chapter 8 goes into the mechanical construction of E-systems while appendices A and B contain the E-BUS pin-out and design check list. An index concludes the handbook.

1.3 MODULE ABBREVIATIONS

In the E-BUS System Design Handbook the short forms in table 1.1 are used for functional component groups (modules).

Type	Abbreviation	Meaning
MICRO-COMPUTER	MC-Module	Microcomputer Module
	MMC-Module	Multi-Microcomputer Module
MEMORIES	MEM-Module	Memory Module
	SRAM-Module	RAM-Memory Module
	EPROM-Module	EPROM-Memory Module
	DRAM-Module	Dynamic-Memory Module
	MBM-Module	Magnetic-Bubble Module
	MIO-Module	Memory and I/O Module
PERIPHERAL CONTROLLER	ICOM-Module	Intelligent Communication Controller Module
	IFDC-Module	Intelligent Floppy Disc Controller Module
	IDSC-Module	Intelligent Disc Controller Module
	IVDU-Module	Intelligent Video Controller Module
	IIEC-Module	Intelligent IEEE Controller Module
	CCM-Module	Communication Controller Module
	MCC-Module	Multi Channel Communication Contr. Module
	FDC-Module	Floppy Disc Controller Module
	VDU-Module	Hard Disc Controller Module
	VDU-Module	Video Controller Module
	CAS-Module	Digital Cassette Controller Module
	IEC-Module	IEEE Controller Module
INPUT/ OUTPUT	OUT-Module	Output Module
	IN-Module	Input Module
	IO-Module	Input/Output Module
	UIO-Module	Universal Input/Output Module
	CTC-Module	Counter/Timer Controller
	AI-Module	Analog Input Module
	AO-Module	Analog Output Module
	AIO-Module	Analog Input/Output Module
	LAI-Module	Low Level Analog Input Module

Table 1-1 Abbreviations for Functional Modules

SECTION 2

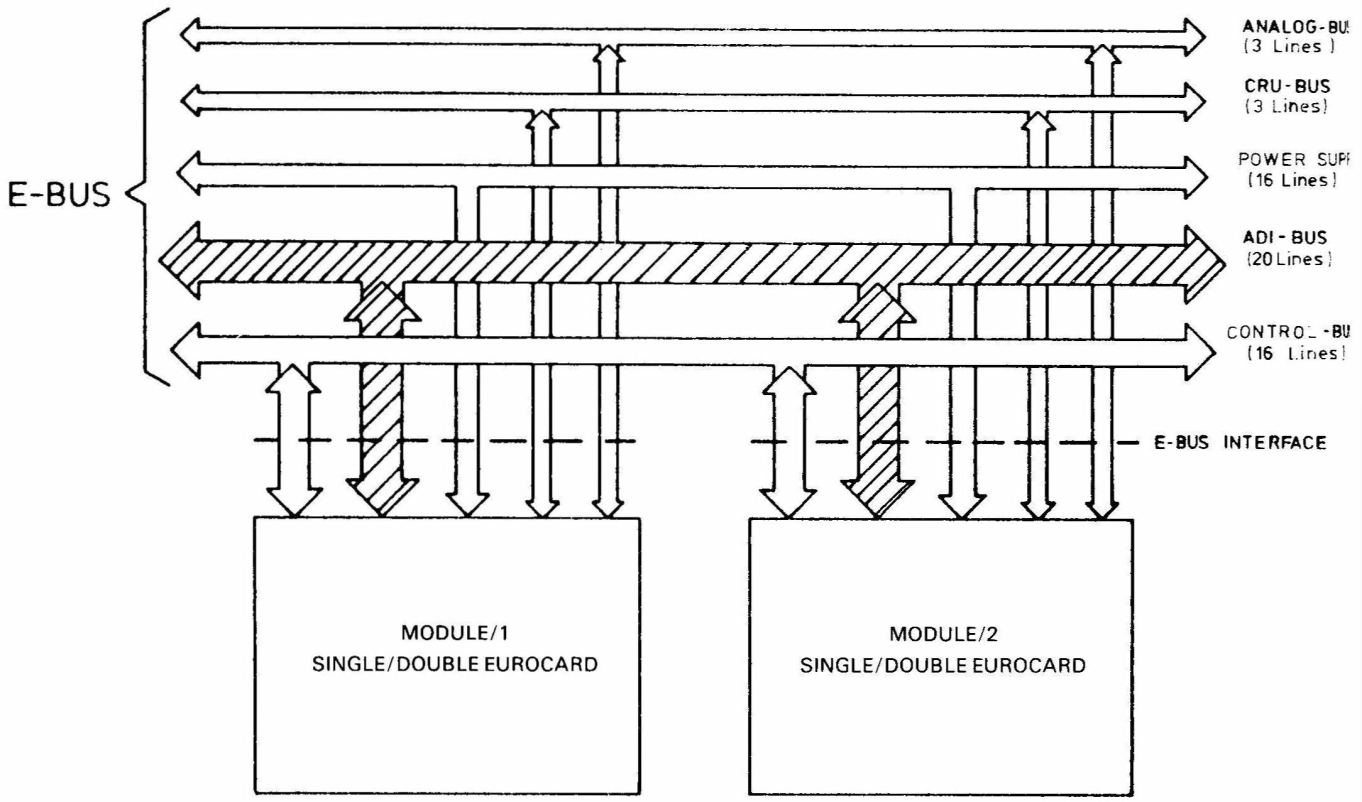
E-BUS DESCRIPTION

The following section gives detailed descriptions of the E-BUS logical and electrical specifications.

2.1 FEATURES

E-BUS serves as a systems interface (see Fig. 2-1) for coupling modular components on single or double Eurocard format and has the following features:

* microprocessor-independent systems interface
* 64 pin DIN 41612 connector (Form C)
* Complete multiprocessor interface
* Multiplexed address, data, and interrupt bus
* 1M byte memory address space
* 8 or 16 bit wide data bus
* Up to 128 interrupts in multiprocessor systems (8 multiprocessors each with 16 interrupt levels)
* Efficient bus control via daisy chain structure
* 2 non-maskable system interrupts (NMI-, PRES-)
* Single interrupt line for power failure (PWRFAIL-)
* Three flexible input/output interfaces (memory mapped I/O, DMA, and programmable CRU input/output)
* Two supply lines for "Stand-By" operation (+5VSTBY and +BATT)
* Five supply voltages (5V, +/-12V and +/-15V)


E-BUS
ANALOG-BU
(3 Lines)
CRU-BUS
(3 Lines)
POWER SUP
(16 Lines)
ADI-BUS
(20 Lines)
CONTRO -BU
(16 Lines)
E-BUS INTERFACE
MODULE/1
SINGLE/DOUBLE EUROCARD
MODULE/2
SINGLE/DOUBLE EUROCARD

2.2 APPLICATIONS

E-BUS was developed specifically for microprocessor applications within the industrial environment. The compact nature, yet with full multi-processor capability with only 64 bus lines, guarantees high reliability and complete integration capability using VLSI technology (VLSI = Very Large Scale Integration).

The following requirements of the industrial environment are relevant to the definition of E-BUS:

* Reliable connectors to DIN 41612
* Standard card format enabling single and double Eurocard boards to be mixed giving optimum modularity of I/O
* Standardised mechanical design to DIN standard
* High performance interrupt structure in multiprocessor systems
* Flexible and cost effective input/output structures for simple or complex applications
* Modular structure: simple 8 bit applications without multiprocessor capability up to complex 16 bit applications with complete multiprocessor structure and large memory address space
* Safe operation on power failure with battery back up or non-volatile memory systems
* Capability for future expansion using reserved pins (7 lines reserved on 64 pin and 39 lines on the 96 pin DIN connector)

E-BUS follows the trend toward small compact microprocessor systems resulting from the increasing density of integration of semiconductor components. In the last ten years the physical space requirements for a 16 bit computer having 64k bytes of memory have been reduced by a factor of 30.

The flexibility and efficiency of E-BUS allows it to be used in the following applications:

- General sequential control
- Machine control - e.g. NC machines
- Robot control for manufacturing automation
- Decentralised process control systems
- Decentralised data acquisition systems
- Process automation
- Laboratory automation
- Regulation systems - e.g. heating controls
- General equipment control in medicine, chemistry, computer peripherals, or measurement technology
- Intelligent terminals, e.g. graphics systems or fast printers

2.3 SIGNAL DESCRIPTIONS

E-BUS comprises the following 6 types of signal:

* Supply voltages:
  - For the supply of digital and analogue modules
* Bus control:
  - For single and multiprocessor systems
* ADI Bus:
  - Multiplexed address, data and interrupt bus
* Control lines:
  - Memory control, system control signals and system interrupts
* CRU Bus:
  - Bit serial input/output interface of the 99XXX microprocessors
* Analogue Bus:
  - Lines for the connection of analogue devices
* Reserved Lines

Table 2-1 gives all E-BUS signals, signal type and pin assignment on the 64 pin DIN 41612, form C, connector.

In the following sections the function of all the E-BUS signal lines is described.

Pin No.	Row A	Signal type	Row C	Signal type
1	GND	Supply line	GND	Supply line
2	PRES-	Control line	BUSCLK-	Bus control
3	+12V	Supply line	-12V	Supply line
4	IORST-	Control line	NMI-	Control line
5	+5V	Supply lines	+5V	Supply line
6	+BATT			
7			Reserved	
8	Reserved			
9				
10	INTEN-	Control line	ALATCH	Control line
11	XA0		XA1	
12	XA2		XA3	
13	A0/D0/INT0		A1/D1/INT1	
14	A2/D2/INT2		A3/D3/INT3	
15	A4/D4/INT4	ADI-BUS	A5/D5/INT5	ADI-BUS
16	A6/D6/INT6		A7/D7	
17	A8/D8		A9/D9	
18	A10/D10		A11/D11	
19	A12/D12		A13/D13	
20	A14/D14		A15/D15/CRUOUT	
21	AREADY-	Control lines	MEMEN-	Control
22	DEN-		READY-	lines
23	GRANTIN	Bus control	GRANTOUT	Bus
24	PWRFAIL-	Control line	BUSY-	control
25	GND	Supply lines	GND	Supply line
26	+15V			
27	ANACOM	Analogue bus	ANAHI ANALO	Analogue bus
28	-15V	Supply line	CRUIN	CRU bus
29	WE-	Control line	+5VSTBY	
30	+5V	Supply line	+5V	Supply lines
31	MEMWIDTH	Control line	CRUCLK-	CRU bus
32	GND	Supply line	GND	Supply line

Row B reserved

Table 2-1 E-BUS Signal Types and Pin Assignment

2.3.1 SUPPLY VOLTAGES

The various supply voltage lines feed all the E-BUS modules with regulated voltages. In general E-BUS modules should only use the +5V supply. The +/-12V supplies are for interface devices, e.g. RS-232C driver. The +/-15V supply may be used to power analogue devices. Within an E-BUS rack the loading on the +/-12V and +/-15V should not exceed 1A per supply.

In total, the E-BUS provides for the following supplies:

Voltage	Number of E-BUS Connections
+5V	4
+5VSTBY	1
+BATT	1
+12V	1
-12V	1
+15V	1
-15V	1
GND (earth)	6

The +5VSTBY and +BATT are provided to supply battery back up memory and real time modules.

These two lines have the following functions:

+5VSTBY:

- The +5VSTBY (STANDBY) supply line maintains its voltage within the prescribed tolerance (+/-3%) even on mains failure. It allows continuous operation of logic requiring a nominal +5V, for example refresh circuits for dynamic memory systems. Within the system the loading of the +5VSTBY line should not exceed 1A.

+BATT:

- The +BATT (battery) supply line is provided for systems which require a battery backup supply voltage other than 5V. For example it may be used to supply CMOS memory modules or a real time clock or to guarantee non-volatile storage of data even on mains failure. It is recommended that the +BATT voltage is selected to have a nominal value of 3.6V since this results in the guaranteed operation of CMOS RAMs (VCC > 2.4V). Within the system loading of the +BATT line should not exceed 1A.

Changeover from mains to battery backup system operation and vice versa is controlled by the signals PWRFAIL- and PRES- (see section 2.3.4).

Notes for the design of battery backup memory modules can be found in section 4.7. Design rules for the construction of the back plane assembly are contained in section 2.5.4 and Appendix B.

2.3.2 BUS CONTROL

Different master modules can gain control over the E-Bus to execute bus operations such as : memory, I/O, DMA, or interrupt transfers. Reliable operation requires signals to indicate the bus status, prioritisation of simultaneous bus requests, and rules for arbitration and release of the E-Bus.

The following signals are provided on the E-Bus for bus control:

- BUSCLK- : Bus Clock (active LOW)
- BUSY- : Bus Busy (active LOW)
- GRANTIN : Access Grant In (active HIGH)
- GRANTOUT: Access Grant Out (active HIGH)

These signals are defined as follows:

BUSCLK-:

- BUSCLK- is the constant system clock. All bus control operations are synchronised with the positive edge of the clock (LOW to HIGH). BUSCLK- is produced by a microprocessor module or an independent clock generator and the frequency must not exceed 10MHz. In a multi-microcomputer system BUSCLK- can be asynchronous to the local microprocessor clock.

BUSY-:

- BUSY- is a bidirectional signal which when active LOW signifies that a module has control of E-BUS. If BUSY- is inactive (HIGH), then no bus operation is taking place at that time. BUSY- is switched to active LOW by the module which has mastery of E-BUS and is driven using either open collector or 3-state gates. If there is no module active on the bus, BUSY- is pulled HIGH by the terminating resistor on the back plane.

GRANTIN:

- When active (HIGH) GRANTIN signifies that no module of a higher priority is requesting the bus. Modules wishing to take control of the bus must evaluate GRANTIN and BUSY- before arbitration of the bus can occur. The GRANTIN input to a module is the GRANTOUT output of the module with the next highest priority. If a module grant line becomes inactive (LOW) it must set its GRANTOUT line inactive with a minimal delay. The GRANTIN line on a module must have a pull up resistor to VCC. On slave modules which never require access to the bus GRANTIN and GRANTOUT should be joined.

GRANTOUT:

- When active (HIGH) GRANTOUT signifies that modules having a lower priority can acquire the bus. Should an internal bus acquisition request occur on a module, the GRANTOUT line must go inactive in synchronism with BUSCLK- to block any bus acquisition by a module of lower priority. GRANTOUT can be driven by either an open collector gate (pull up resistor on module) or an active output (totem pole).

2.3.2.1 PRIORITY DETERMINATION

The priority of a module within an E-BUS system is determined by reference to the GRANTIN/GRANTOUT line. Priority determination may take two forms :

- serial (DAISY CHAIN) or
- parallel priority control

E-BUS supports serial priority control using the daisy chain principle, which will be described in detail below.

Since the specification of a bus acquisition ensures that priority determination is transparent, parallel priority control can also be used in special applications. An advantage of serial priority control is that no additional hardware is needed. Parallel bus arbitration requires additional hardware. (see section 3.2.2).

In serial priority control, the individual slots in a chassis are assigned a fixed priority. As shown in Fig. 2-2, at each slot the GRANTOUT line on one module is connected to the GRANTIN line of the next module. This results in a linear sequence of priorities which decreases from left to right, slot 1 (leftmost) having the highest priority, since its GRANTIN line is pulled HIGH via the pull up resistor on the module.

The other signals required for control of the bus, BUSY- and BUSCLK-, are available to each slot in parallel.

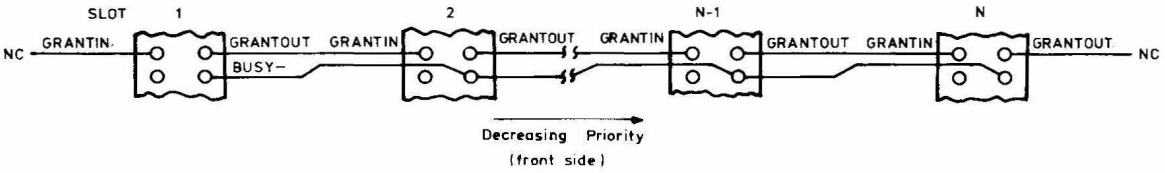


Figure 2-2 E-BUS Serial Priority Assignment

For correct operation of the serial priority chain, the GRANT lines must not be broken, which means that there must be no empty slots between the boards in a system. If this is not possible, then on any free slot between boards, GRANTIN and GRANTOUT must be connected, e.g. joined using jumpers on the back plane.

2.3.2.2 BUS ARBITRATION

The GRANTIN line, together with the BUSY- line (which signifies occupation of E-BUS), essentially controls a bus acquisition. Fig. 2-3 shows a flow diagram of the bus arbitration. If an internal bus request occurs on a module then the GRANTOUT line is set to a LOW level, clocked synchronously with BUSCLK-. Thereafter the states of BUSY- and GRANTIN are evaluated on each positive edge of BUSCLK-. If the E-BUS is not occupied (BUSY- at HIGH level) and GRANTIN is active (HIGH level) then acquisition of the bus can occur by activating the BUSY- line.

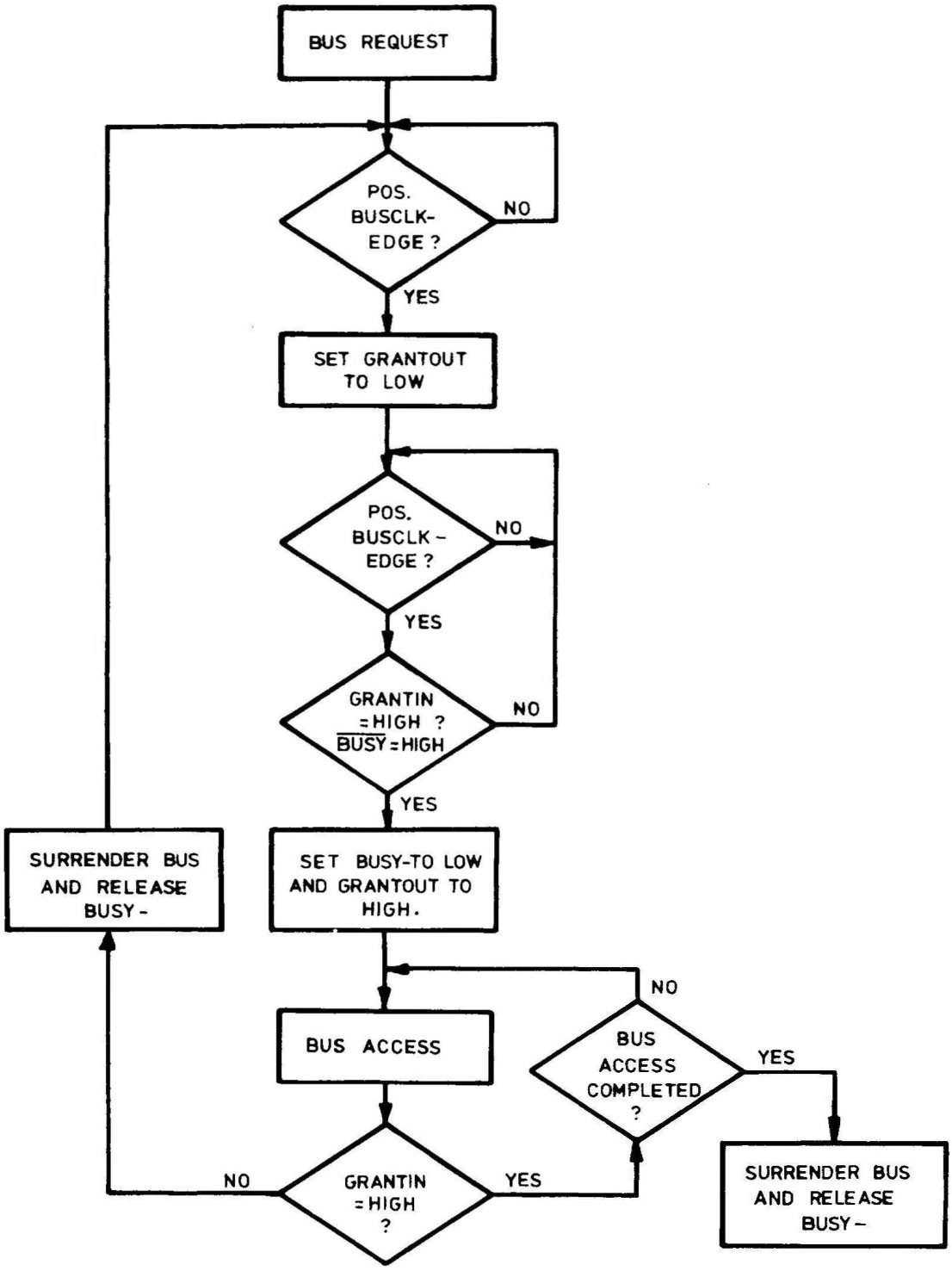


Figure 2-3 Flow Diagram of a Bus Arbitration

If BUSY- is active or GRANTIN inactive then acquisition of the bus must be delayed until the E-BUS is free and no higher priority module has requested access.

If a module has mastery over E-BUS and another module of higher priority requests the bus (GRANTIN becomes inactive) then the bus must be released after the present cycle has been executed. The only exception to this rule is in the case of a particular cycle which must not be interrupted, for example, testing and setting of system flags (semaphores) in multi-microcomputer operation (see section 3.5.3). Fig. 2-4 shows the timing diagram of a module forcing re-arbitration of the bus. If the module assumes mastery of the bus, then GRANTOUT can be set active HIGH again synchronously with BUSCLK- since BUSY- is active and no other module can occupy E-BUS.

Once control of the bus is to be concluded, then E-BUS is released on the next positive edge of BUSCLK-.

In order to achieve a fast exchange of bus control BUSY- must be released as early as possible during the last BUSCLK- cycle. The next bus arbitration can then take place on the subsequent positive edge of BUSCLK-.

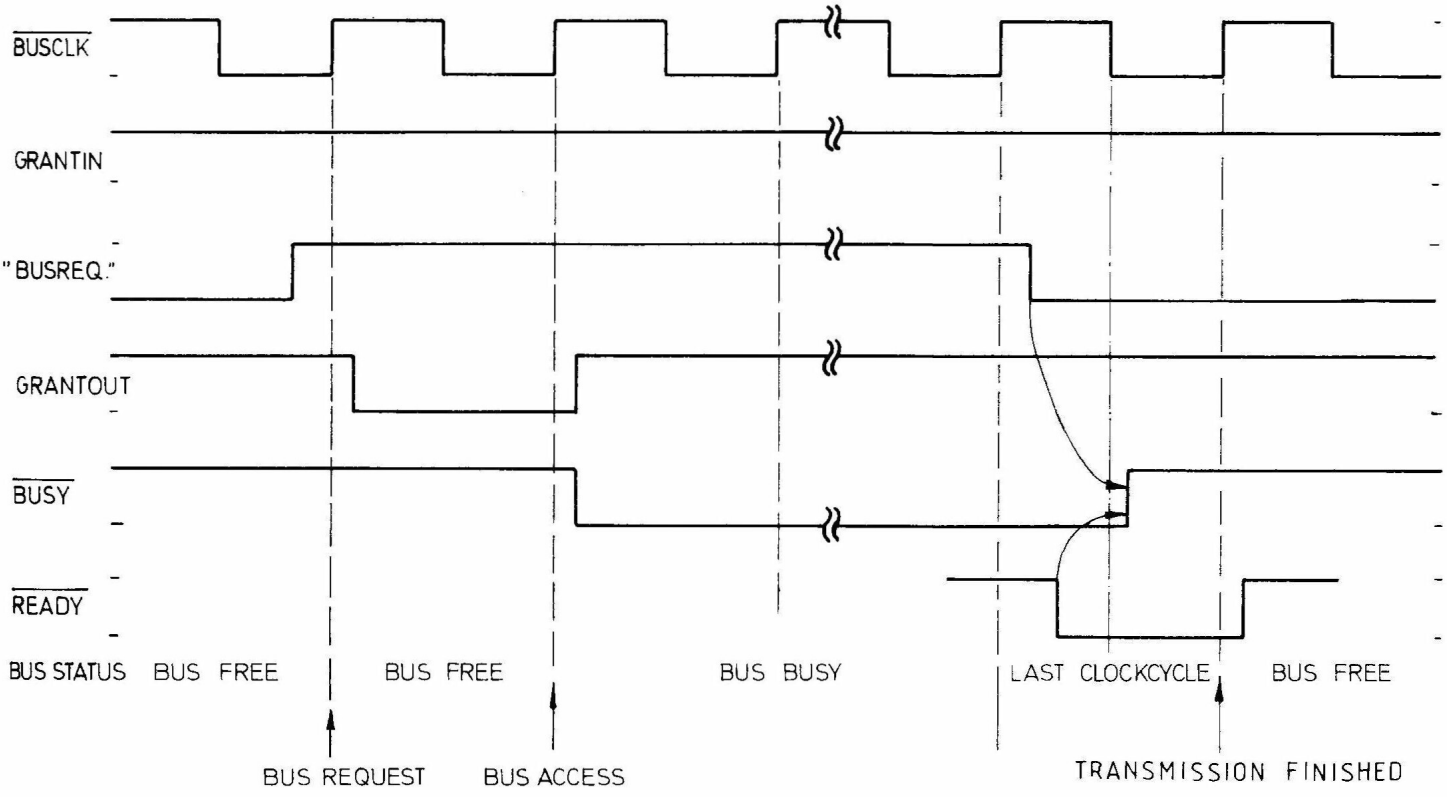


Figure 2-4 Bus Arbitration Timing Diagram

2.3.2.3 BUS CONTROL WITH MULTIPLE MODULES

In order to further explain the concept of priorities, a timing diagram is developed relating to prioritised bus arbitrations by two or three modules. In the first example the E-BUS is occupied by a module which is interrupted by a module of higher priority. Fig. 2-5 shows the relevant timing diagram of the GRANT, BUSREQ, BUSY- and READY- lines. While module 2 occupies the bus, a bus arbitration is requested internally on module 1 (bus request [M1]). Following this request the GRANTOUT line of module 1 (GRANTIN of module 2) is set LOW synchronously with BUSCLK-. The memory cycle which was being performed by module 2 is completed (READY- goes LOW) and E-BUS is released (GRANTOUT of module 2 remains inactive LOW). On the next positive edge of BUSCLK- module 1 occupies E-BUS, BUSY- goes LOW and GRANTOUT (M1) HIGH. Module 1 bus mastery terminates when its internal bus request goes LOW. BUSY- then goes HIGH on the following negative edge of BUSCLK- corresponding to the completion of the memory cycle (READY- goes LOW). On the next positive edge of BUSCLK- module 2 can once again occupy E-BUS.

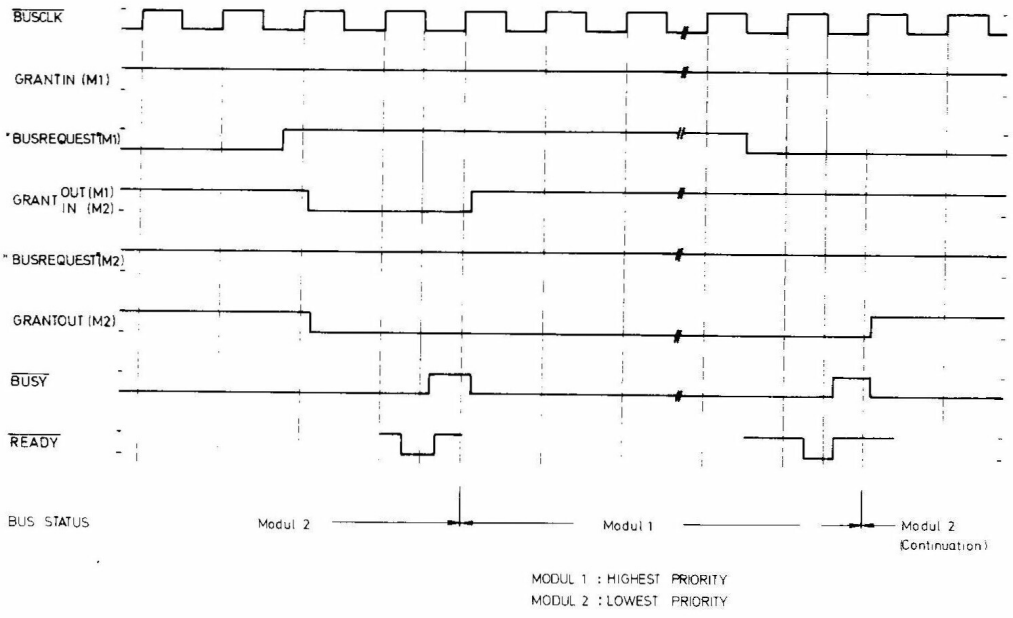


Figure 2-5 Bus Control with Two Modules

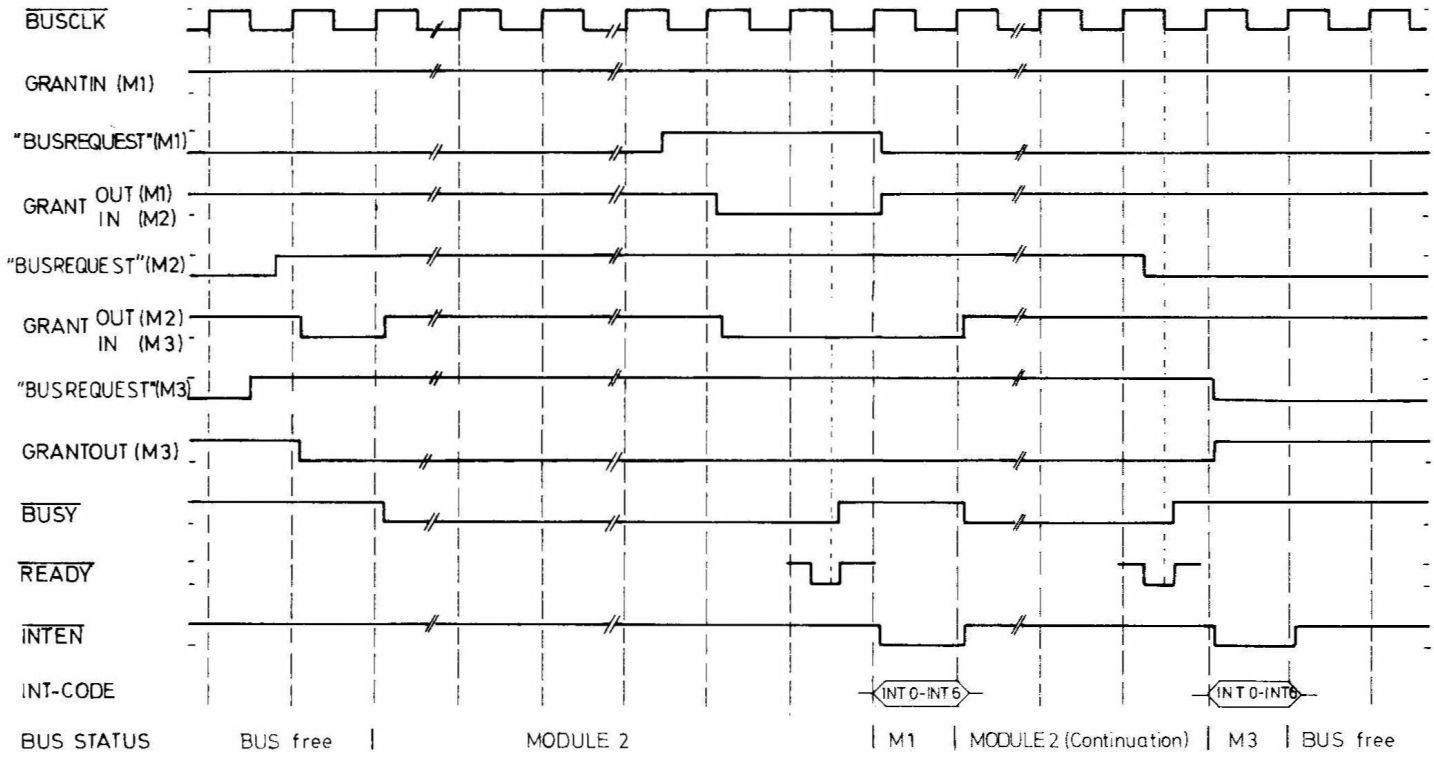
The next example assumes the following situation;

- E-BUS module 1 (interrupt module with highest priority), module 2 (processor module with medium priority) and module 3 (interrupt module with lowest priority) are all capable of mastery of the bus.
- Modules 2 and 3 receive an internal bus request virtually simultaneously.
- Module 2 has control over the bus and is interrupted by module 1 for an interrupt cycle. It then accesses the bus again to complete its required bus operations.
- Module 3 occupies the E-BUS once it becomes free and no request of a higher priority exists.

Fig. 2-6 shows the timing diagram for this example. After the first BUSCLK- cycle the GRANTOUT line is set LOW by the internal bus requests of modules 2 and 3; on the next positive edge of BUSCLK- module 2 acquires the E-BUS since it has a higher priority than module 3 (GRANTIN on module 2 is HIGH). The bus arbitration of module 2 is interrupted by a request from module 1, although module 1 only occupies the bus for one BUSCLK- cycle in order to transmit an interrupt code (INTEN- is LOW).

Any module on E-BUS which can only occupy the bus for one cycle of BUSCLK- need not set BUSY- to LOW. Since module 1 sets its GRANTOUT output HIGH at the beginning of the interrupt cycle, module 2 can acquire the bus again on the next positive edge of BUSCLK-. This so-called "short bus arbitration" ensures that no time is wasted when the bus is being controlled by more than one module. If an interrupt module sets BUSY- LOW, even though it only occupies E-BUS for one BUSCLK- cycle, the subsequent BUSCLK- cycle is lost (see also section 6.3 and 6.4).

After module 2 has concluded its bus transfers, the short bus access cycle of module 3 can occur.



Module 1: highest Priority
Module 2: medium Priority
Module 3: lowest Priority

Figure 2-6 Bus Control with Three Modules

2.3.2.4 BUS OPERATIONS

If a module has assumed control of the E-BUS and has set BUSY- LOW then three different bus operations may be performed:

1. Memory or parallel input/output transfer (memory mapped I/O),
2. Interrupt code transfer or
3. Bit serial input/output transfer (CRU).

Apart from the bit serial input/output transfer (CRU-Communication Register Unit), which is specific to the 99XXX microprocessors, all other bus operations are transparent to

8 and 16 bit microprocessors. Fig. 2-7 shows a state diagram of the three different E-BUS operations.

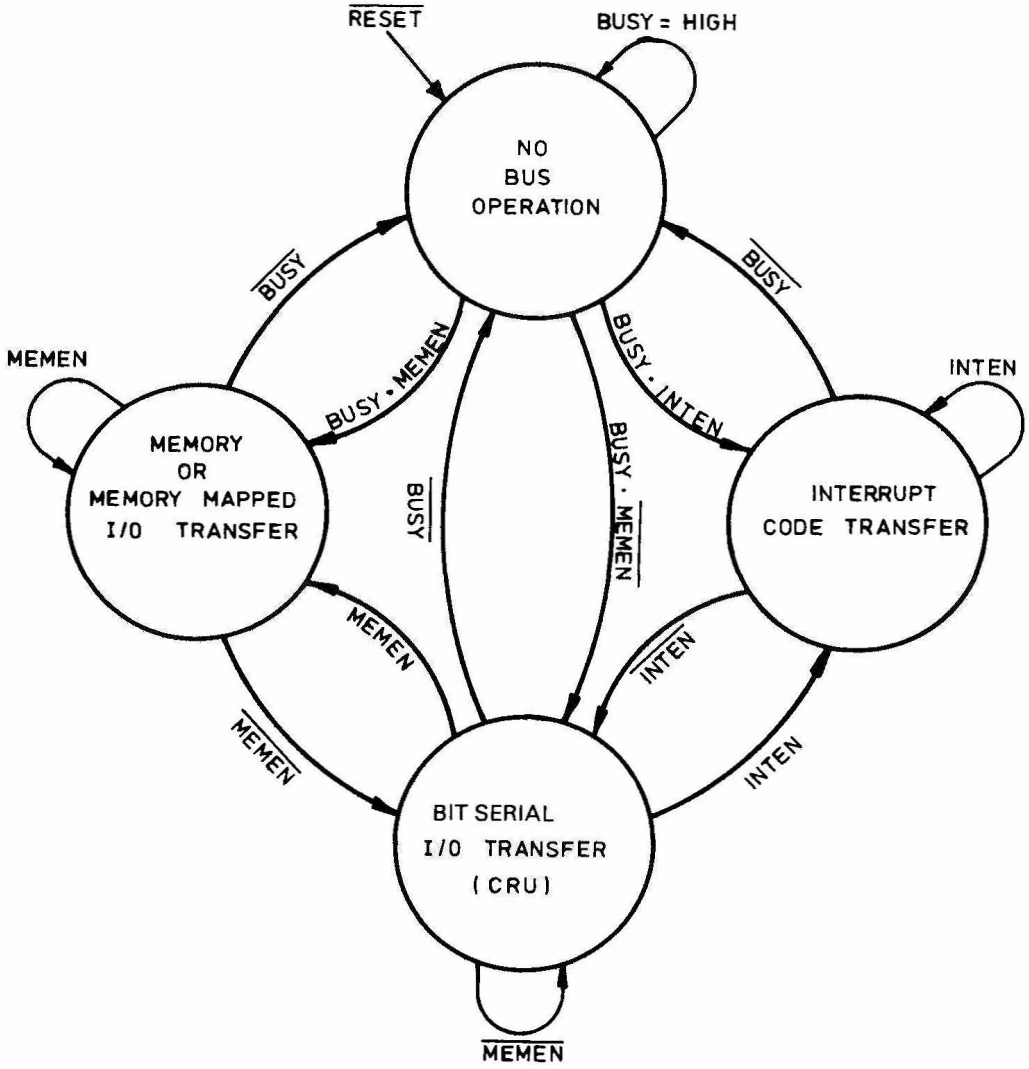


Figure 2-7 State Diagram of E-BUS Operations

2.3.3 ADI AND CRU BUS

On E-BUS, address, data and interrupt information is transmitted in a time multiplexed manner in order to achieve an optimum use of the lines available. Fig. 2-8 shows functions and data flow paths of the multiplexed ADI bus, and table 2-2 shows the truth table for the four primary control lines. On master modules (modules which can take control of the bus), multiplexing of the originally parallel address, data, and interrupts is achieved using 3-state buffers (e.g. SN74LS245 etc.). Slave modules demultiplex the addresses and interrupts via transparent registers (e.g. SN74LS373 latches). Data lines require only a 3-state buffer. The bit

serial input/output (CRU) uses the ADI bus for address transmission (address of the ingoing or outgoing I/O bits), and also A15/D15/CRUOUT as a bit serial data output line. The ADI bus control lines MEMEN, ALATCH and INTEN- are HIGH for CRU operations.

FUNCTION	CONTROL LINES (BUSY-= LOW)			
	MEMEN-	ALATCH	INTEN-	CRUCLK-
ADDRESS TRANSFER	LOW	HIGH	HIGH	HIGH
DATA TRANSFER	LOW	LOW	HIGH	HIGH
INTERRUPT TRANSFER	HIGH	HIGH	LOW	HIGH
BIT SERIEL INPUT	HIGH	HIGH	HIGH	HIGH
BIT SERIEL OUTPUT	HIGH	HIGH	HIGH	LOW

Table 2-2 ADI Bus Control Lines Truth Table

The expense of interface components is not increased by the multiplexing/ demultiplexing on the ADI bus; it merely requires different components (latches instead of simple buffers). Since memory devices have access times in the order of 70-450ns, multiplexing of address and data results in no loss of speed during a memory transfer. Fig. 2-9 shows memory and interrupt cycles occurring on the ADI bus, in schematic form.

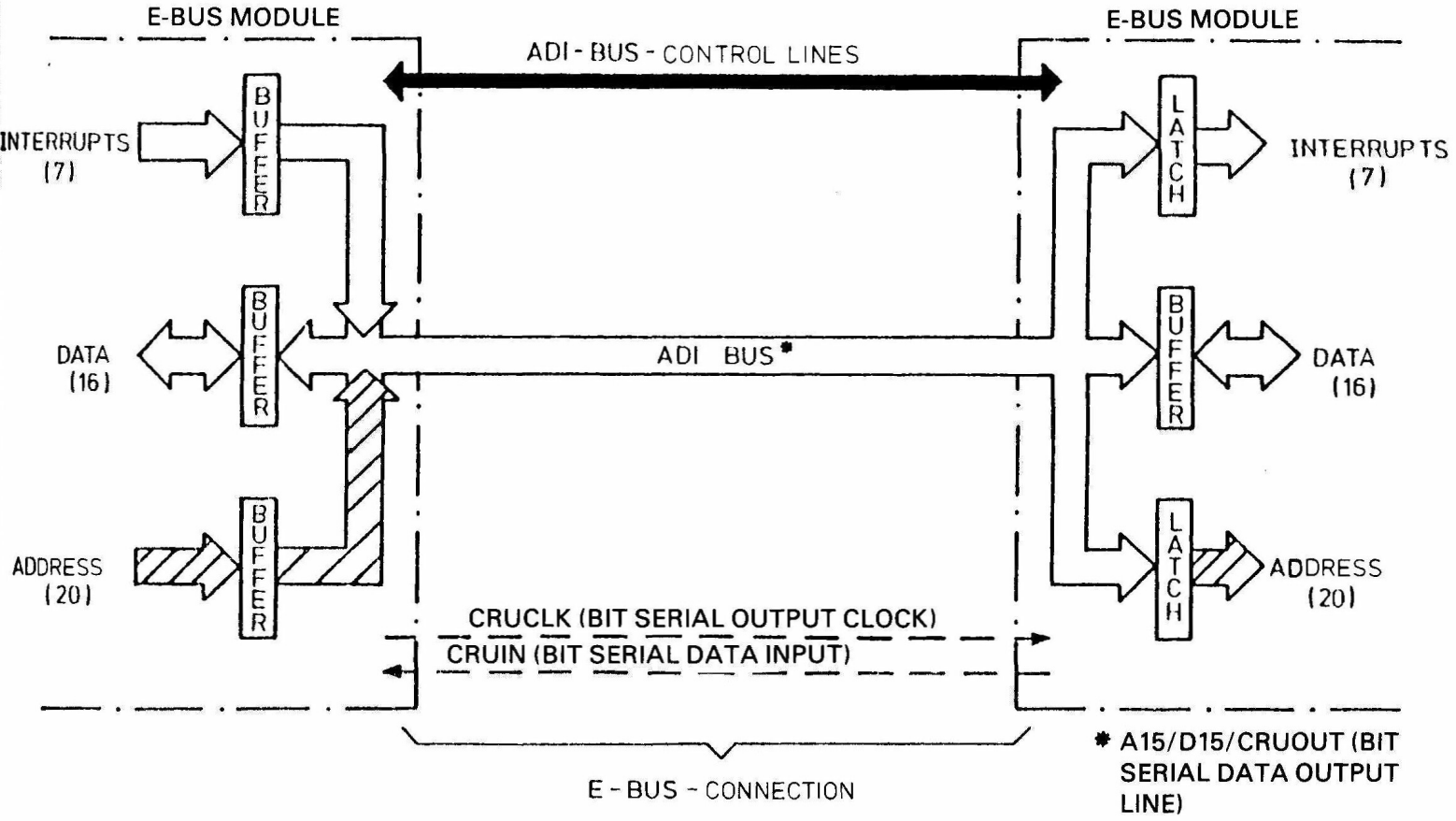


Figure 2-8 ADI and CRU Bus Data Paths

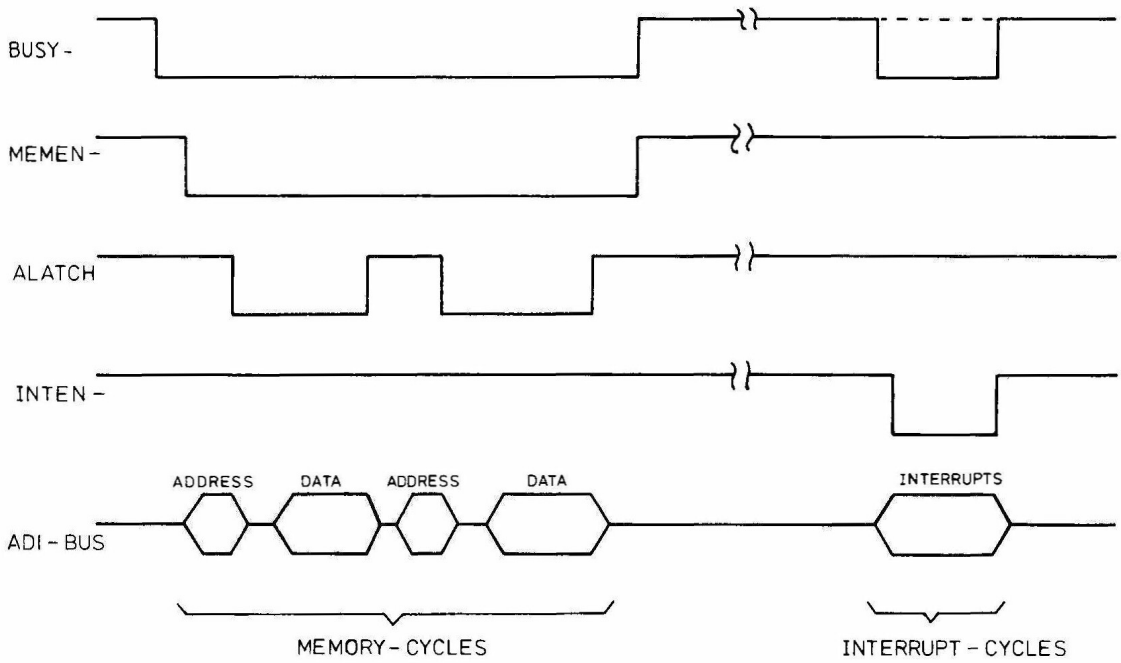


Figure 2-9 ADI Bus Multiplex Timing

2.3.3.1 MEMORY TRANSFER SIGNALS

The transmission of data from memory or parallel input/output (memory mapped I/O) may be controlled (for example) by a microprocessor or a DMA module on E-BUS. The relevant memory transfer signals are given below:

* Address and data lines A0/D0/INT0 to A15/D15/CRUOUT and the extended address lines XA0 to XA3.

* Control lines MEMEN-, ALATCH, DEN-, WE-, MEMWIDTH, READY- and AREADY-

These signals are defined as follows:

* A0/D0/INT0 to A15/D15/CRUOUT:

  - The multiplexed 16 address and data lines A0/D0/INT0 (MSB) to A15/D15/CRUOUT (LSB) are bidirectional bus lines. The 16 address bits (A0-A15) are transmitted when ALATCH is HIGH, and with ALATCH LOW 16/8 data bits (D0-D15) are transmitted. The direction of the transmission of data is controlled by the signals DEN- and WE-.

* XA0-XA3:

  - The four extended address bits XA0 (MSB) to XA3 (LSB) are bidirectional bus lines and produce a 20 bit wide address bus. It is thus possible to address up to 1M byte or 512k 16 bit words. The extended address lines are only used for address transmission.

* MEMEN-:

  - MEMEN- (MEMory ENable) being active (LOW) signifies that a memory read or write operation is in progress. MEMEN- is controlled by the module which has mastery of the bus and can be active over several successive memory operations. If MEMEN- is inactive (HIGH) then CRU input/output operations can be performed. MEMEN- is a bidirectional bus line and hence must be controlled by a 3-state driver.

* ALATCH:

  - If ALATCH (Address LATCH) is active (HIGH) it signifies that a memory or CRU address is on the ADI bus. The negative edge of ALATCH is synchronised with the positive edge of BUSCLK- and is used to store address information in the address register (latches) on memory or parallel input/output modules. If ALATCH is LOW, data is being transmitted on the ADI bus. During CRU input/output operations ALATCH remains HIGH. ALATCH is a bidirectional bus line and hence must be controlled by a 3-state driver on the current bus master.

* DEN-:

  - If DEN- (Data driver ENable) is active (LOW) this signifies a read cycle from memory or input/output module to the master module. With DEN- set LOW, the addressed memory or input/output module can output its data to the ADI bus. DEN- is a bidirectional bus line and hence must be controlled by a 3-state driver on the module which is the current master of E-BUS.

* WE-:

  - If WE- (Write Enable) is active (LOW) then this signifies that transmission of data on the ADI bus from the microprocessor or DMA module (current Bus master) to memory or input/output module is in progress (write cycle). WE- is a bidirectional bus line and hence must be controlled by a 3-state driver on the module which has mastery of E-BUS.

* MEMWIDTH:

  - MEMWIDTH (MEMory WIDTH) indicates whether a byte (8 bit) or a word (16 bit) transfer occurs during a memory or parallel input/output cycle. If MEMWIDTH is HIGH then a byte transfer is in progress. A LOW level signifies a word transfer. Memory or parallel input/output modules use MEMWIDTH to control the corresponding interface circuitry for byte or word transfers. MEMWIDTH is a bidirectional bus line and hence must be controlled by a 3-state driver on the current master module.

* READY-:

  - The READY- signal indicates that, when active (LOW), the memory cycle can be concluded in the current BUSCLK- cycle. READY- is controlled from the addressed memory or input/output module via a 3-state or open collector output. A HIGH (inactive) state is guaranteed by terminating resistors on the back plane.

* AREADY-:

  - The AREADY- (Advanced READY) signal indicates, when active (LOW), that the memory cycle can be concluded after the next (!) BUSCLK-cycle. AREADY- is provided for micro-processors which require an "advanced warning" ready signal from memory. All of the conditions for AREADY- are identical to those for READY-.

A complete synchronous memory read and write cycle for a single master is shown in figure 2-10. It was assumed that the MC-module uses a microprocessor which requires a minimum of two BUSCLK- cycle for a complete memory transfer and therefore uses the AREADY- signal (without wait states).

A MC-module on which the microprocessor can complete a memory transfer with one BUSCLK- cycle, like the TM990/E155 MC-Module, uses READY-. The number of wait states required depends on the access time of the memory chips used.

The timing of parallel I/O transfer is identical to the memory cycle.

The realisation of memory modules is described in detail in section 4.

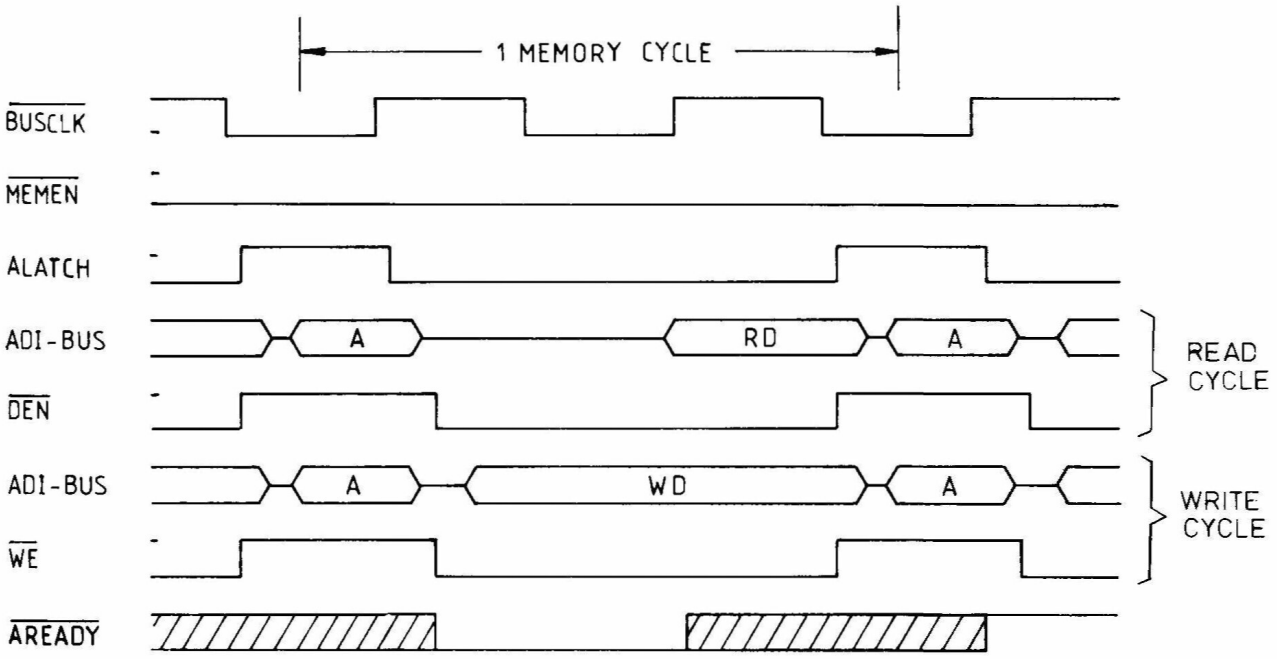


Figure 2-10 Memory Cycle Timing Diagram

2.3.3.2 INTERRUPT TRANSFER SIGNALS

On E-BUS an interrupt code can be transmitted by various modules (e.g. microprocessor, input/output or memory modules) once the module has achieved control of the bus by means of the E-BUS control signals. The following interrupt transfers may occur on E-BUS:

- interrupt between multi-microcomputer modules
- interrupt between I/O and microcomputer or multi-microcomputer modules
- interrupt between autonomous I/O control units (e.g. between floppy disc control and DMA module).

Only the INTEN- line (INTerrupt ENable) is required to be controlled in addition to the bus control signals (see section 2.3.2) and the ADI bus lines A0/D0/INT0 to A6/D6/INT6.

Once a module wishing to transmit an interrupt code has gained control of E-BUS the interrupt transfer is performed within one BUSCLK- cycle.

The lines for the interrupt transfer are defined as follows:

* A0/D0/INT0 to A6/D6/INT6:

  - During an interrupt cycle these 7 ADI bus lines transmit the 4 bit code for the interrupt level (INT3 [MSB] to INT6 [LSB]) and the 3 bit code for the MMC-module address (INT0 [MSB] to INT2 [LSB]). With a maximum of 8 MMC-modules, this gives 128 possible interrupt levels.

* INTEN-:

  - The active (LOW) state indicates that transmission of the interrupt code is occurring on lines A0/D0/INT0 to A6/D6/INT6. INTEN- is controlled by that module which has control over E-BUS and is active for a maximum of one BUSCLK- cycle. It is a bidirectional bus line which must be driven by a 3-state or open collector output.

Fig. 2-11 shows an interrupt transfer together with the required bus control.

As already explained in the second example in section 2.3.2.3, BUSY- need not be activated for the short interrupt cycle. If a master module wants to occupy the E-BUS for more then one BUSCLK- cycle it must pull the BUSY-line to LOW.

The interrupt operation of E-BUS systems is described in detail in section 7.

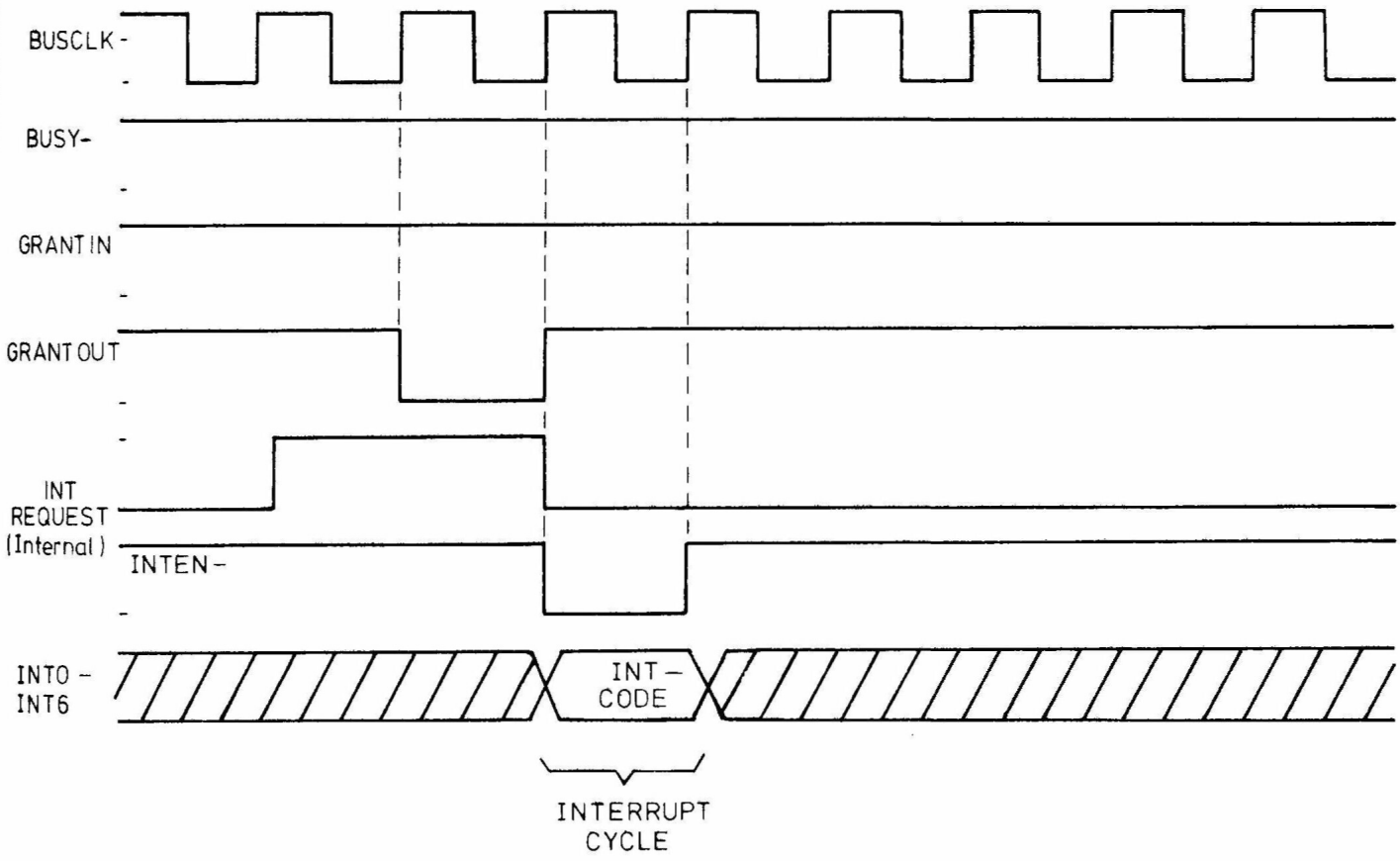


Figure 2-11 Interrupt Transfer Timing Diagram

2.3.3.3 BIT SERIAL INPUT/OUTPUT TRANSFER SIGNALS

The bit serial input/output interface (CRU = Communications Register Unit) uses the ADI bus lines (A3/D3/INT3 to A14/D14 and A15/D15/CRUOUT) for the transmission of the bit address and serial data information. In addition the output clock (CRUCLK-) and the input data line (CRUIN) are required for this interface. In contrast to byte or word memory or parallel input/output transfer, this interface transmits information in bit serial fashion. E-BUS supports up to 4096 input and 4096 output bits via the serial CRU interface.

The relevant signal lines are defined below:

* A3/D3/INT3 to A14/D14:

  - The address lines A3/D3/INT3 (MSB) to A14/D14 (LSB) contain the address of the required input/output bit for bit serial input/output transfer (MEMEN- and ALATCH are HIGH, A0-A2 are LOW). The Address lines are controlled by

the module which has control over E-BUS at the time and is executing a bit serial input/ output transfer.

* A15/D15/CRUOUT:

  - The ADI bus line A15/D15/CRUOUT transfers the data output information during a bit serial output transfer (MEMEN- = ALATCH = HIGH, and CRUCLK- is LOW). During a bit serial input transfer this line is ignored.

* CRUCLK-:

  - When active (LOW) the CRUCLK-line signifies valid data output information on the A15/D15/CRUOUT line. CRU output modules on the system bus should sample the data on the positive edge of CRUCLK-. CRUCLK- is a bidirectional bus line and is controlled by a module which has control of E-BUS. CRUCLK- must be driven by a 3-state output.

* CRUIN:

  - During a bit serial input transfer (MEMEN- = ALATCH = HIGH) the state of the addressed input bits is transmitted from the module to the MC or MMC-module on the CRUIN line (CRU INput). Since an MC or MMC-module only samples the CRUIN line during a bit serial input transfer, a CRU input module need not differentiate between an input or output transfer (CRUCLK- is only evaluated on an output module). CRUIN is a unidirectional bus line and is controlled via a 3-state or open collector output on the module supplying the addressed input bits.

A bit serial input or output transfer consists of the sequential tansmission of 1 to 16 bits. Fig. 2-12 gives a timing diagram for a bit serial input/output transfer.

Chapter 5 describes in detail input/output modules having bit serial CRU interfaces.

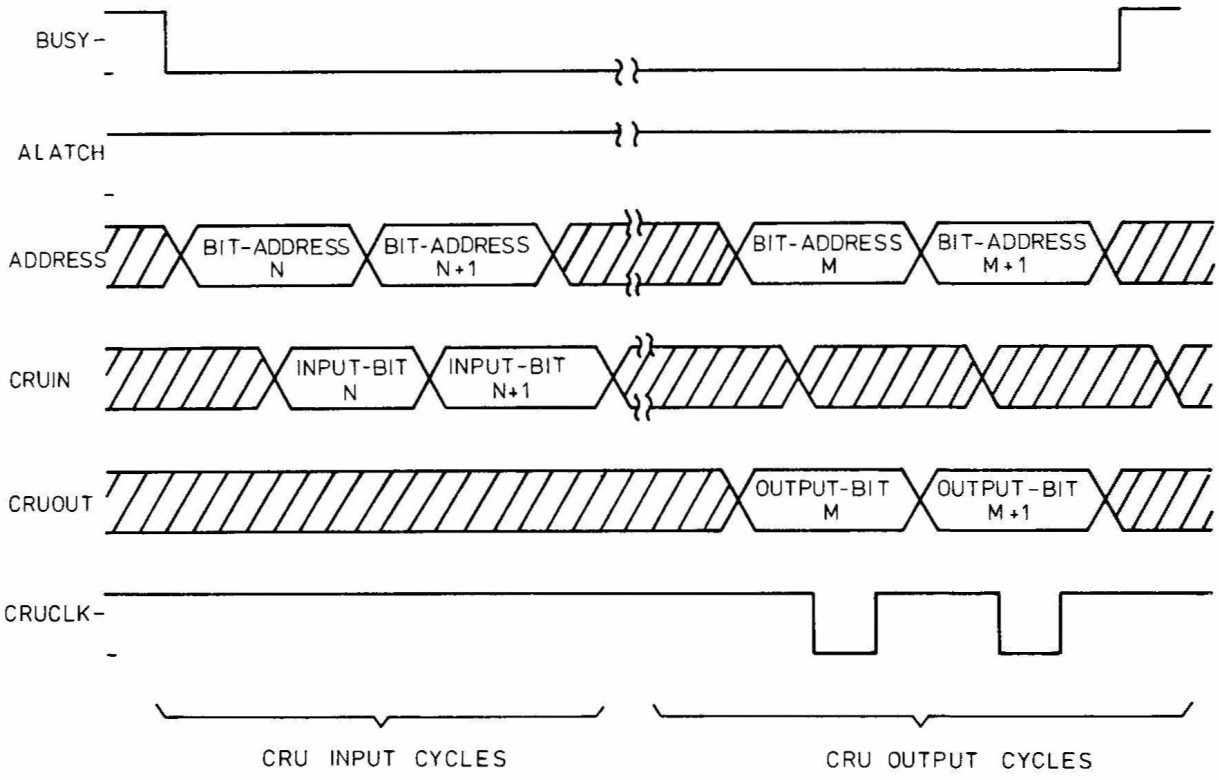


Figure 2-12 Bit Serial Input/Output Transfer

2.3.4 SYSTEM CONTROL SIGNALS

In parallel to the control signals for arbitration on E-BUS, described in section 2.3.2, there exist a number of system control signals which are provided to produce satisfactory powering up and down of an E-system.

2.3.4.1 RESET LINES

The system control lines PRES- (Power on RESet) and IORST- (Input/Output ReSeT) cause an entire E-system and/or all input/output modules to be reset.

These lines are specified below:

* PRES-:

  - The PRES- signal is active LOW and is generated by the mains supply. PRES- remains active during a switch on delay (greater than 100ms) following application of the supply voltages. PRES- being at the HIGH level signifies that all the supply voltages on E-BUS are within their +/-3% tolerance. PRES- must be at a guaranteed LOW level during on/off transients, in the powered down state and during mains failure. PRES- must be controlled by mains logic and must utilise an open collector output. In the inactive state PRES- goes HIGH due to a pull up resistor to Vcc on the back plane.

* IORST-:

  - The IORST- signal is active LOW and is controlled by the MC-module to set all connected input/output modules into a defined state. After an MC-module receives an active PRES- signal, or an internal reset is produced following switch on, IORST- must be active for a minimum of 2 BUSCLK- cycles. Normally IORST- is generated by a microprocessor command (e.g. RSET on all 99XXX microprocessors).

2.3.4.2 SYSTEM INTERRUPT LINES

The control of a cold or warm start of the MC-module programs is facilitated with the E-BUS system interrupt lines NMI- (Non Maskable Interrupt) and PWRFAIL- (Power FAIL).

These signals are defined below:

* NMI-:

  - The NMI- signal is active LOW and produces a non maskable interrupt to all MC-modules connected to E-BUS. After RESET, NMI- is the highest priority interrupt within the microprocessor system. NMI- must be active for a minimum of 100ns and is controlled by an open collector output, the HIGH level being guaranteed by a pull up resistor to Vcc on the back plane. NMI- is used for system initialisation after the initial power up of an E-system (cold start). Another cold start possibility via NMI- is following a system RESET or a system malfunction, e.g. via a supervision circuit (watch dog timer).

* PWRFAIL-:

  - The PWRFAIL- signal is active LOW and is generated via an open collector output by a supervision circuit monitoring mains failure. PWRFAIL- going LOW signifies that the supply voltages are only guaranteed for a further 20ms. The mains supply must include a suitable reservoir capacitor to supply the system for a worst case minimum of 20ms. In E-systems PWRFAIL- is used to guarantee a safe restart of the system once mains power is restored (warm start). On MC-modules, PWRFAIL- must have the highest interrupt priority following RESET and NMI-. In order to recognise even momentary mains failures which do not lead to the loss of supply voltages the PWRFAIL- signal should be monitored by software on MC-modules. A pull up resistor to Vcc on the back plane produces the HIGH level of PWRFAIL-.

For the control of correct data integrity operation within E-systems on mains failure (e.g. battery backed SRAM module, TM990/E251) the signals PRES- and PWRFAIL- are of central significance. Fig. 2-13 shows the relevant timing diagram for the signals for power up and down, and on mains failure. Cold and warm program starts are dealt with in section 3.4.

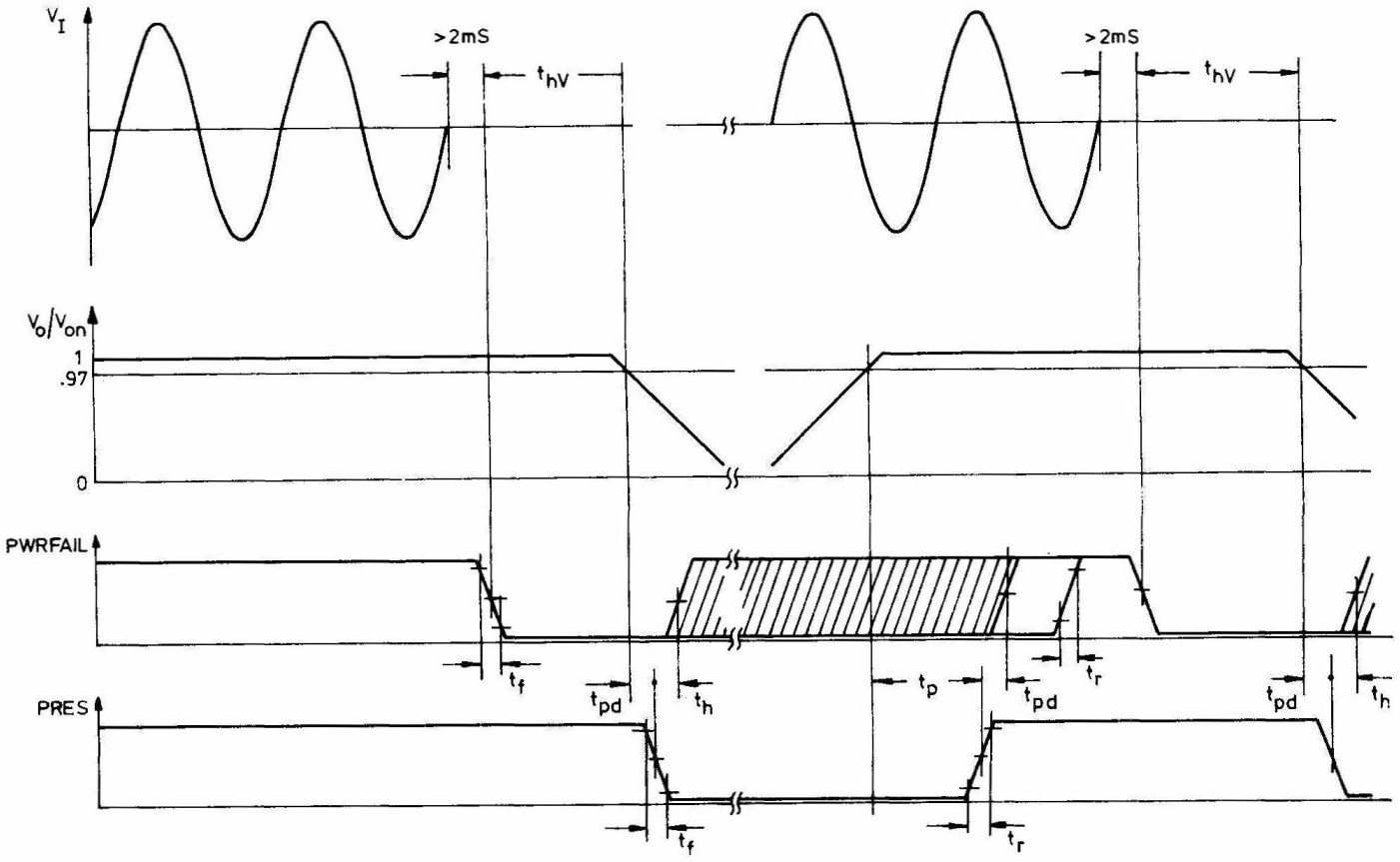


Figure 2-13 PRES- and PWRFAIL- Timing Diagram

2.3.5 ANALOGUE SIGNAL LINES

E-BUS contains three analogue signal lines which are provided to transmit signals which are a maximum of +/-10V relative to analogue ground (ANACOM).

The bidirectional lines ANAHI (ANAlogue HIgh) and ANALO (ANAlogue LOw) are available for the transmission of differential analogue signals. In relation to ANACOM (ANAlogue COMmon) ANAHI is the more positive and ANALO the more negative signal line of the differential transmission.

ANACOM is separated from the digital ground and should be connected to the system earth at a single point.

2.4 RESERVED LINES

For future E-BUS expansion by Texas Instruments, pins A7, 8, 9 and C6, 7, 8, 9, together with all of row B (on the 96 pin connector option) are reserved.

2.5 ELECTRICAL SPECIFICATION

The following sections give the electrical specifications of E-BUS, defining logic levels, signal loading conditions, termination of E-BUS lines, and characteristics of the back plane.

2.5.1 LOGIC LEVELS

E-BUS logic levels are TTL compatible. The static noise immunity is defined to be a minimum of 300mV at a LOW level and a minimum of 400mV at a HIGH level. The logic levels of drivers and receivers on all E-BUS digital signal lines must be within the limits given in table 2-3.

	LOW Level			HIGH Level			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Receiver	0.0	0.4	0.8	2.0	3.4	5.25	V
Transmitter	0.0	0.4	0.5	2.4	3.4	5.25	V

Table 2-3 E-BUS Signal Levels

2.5.2 NOMINAL SIGNAL LOADING

To simplify calculations of E-BUS signal line loading, a standard load is defined (UBL = Unit Bus Load). The direct current requirement of a UBL for a LOW level is standardised to be 0.2mA while that for the HIGH level is 0.02mA (see table 2-4). Loading on an E-BUS signal line is presented by the following:

- line receiver
- line driver in high impedance state for bidirectional lines
- line terminating resistors

From Fig. 2-14, it can be seen that the signal driver source current must be greater than or equal to the total of all "load" currents (sink or termination currents). This is true for both HIGH and LOW levels on the line.

	LOGIC LOW	LOGIC HIGH
UNIT BUS LOAD (UBL)	0.2 mA @ V_{OL} = 0.5V	0.02mA @ V_{OH}=2.4V

Table 2-4 Nominal E-BUS Signal Loading

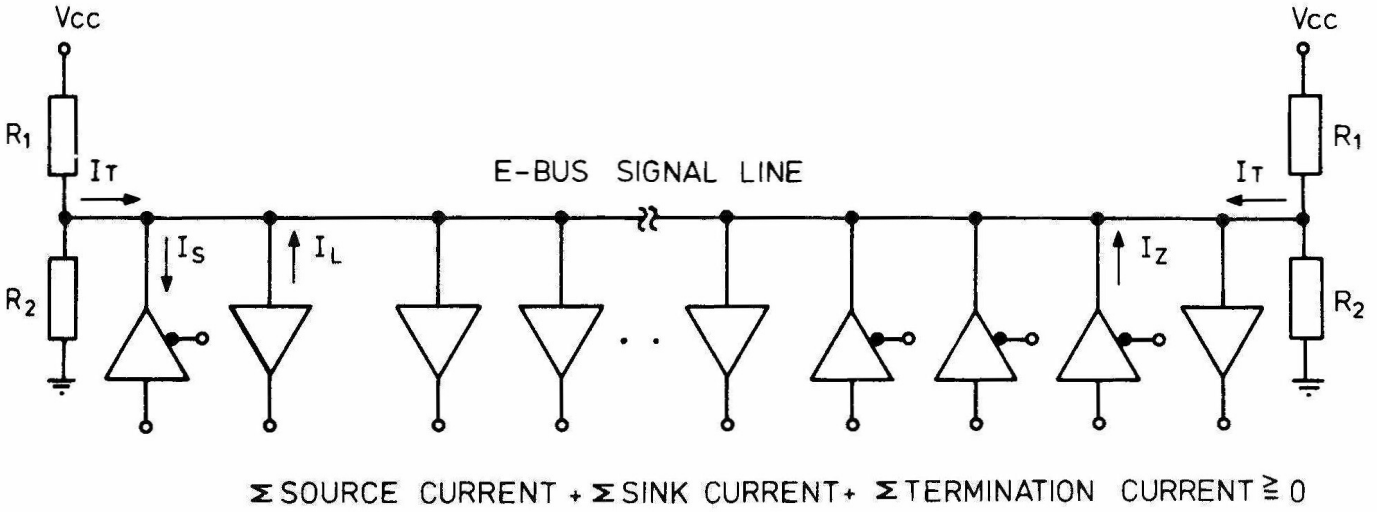


Figure 2-14 E-BUS Signal Line Loading

Currents which flow from the E-BUS signal line are defined as being positive and those which flow into the signal line are defined as negative currents. Therefore SN74S/LS or ALS series driver and receiver currents, as defined in data sheets, can be used directly.

The standard calculation is as follows:

UBLsource + UBLsink + UBLtermination = 0

As an example the SN74LS245N bidirectional driver has the following standardised E-BUS loading:

SN74LS245N	LOW level (Vol=0.5V)	HIGH level (Voh=2.4V)
*driver mode (Iol=24mA,Ioh=-3mA)	120 UBL's	-150 UBL's
*receiver mode (Iil=-0.4mA,Iih=0.02mA)	-2UBL's	1 UBL

Further examples of standardised signal loadings for commonly used driver and receiver devices are given in table 2-5.

		E-BUS Receiver Load		E-BUS Driver Capability		
Type	Function	Low	High	Low	High	Unit
SN74LS00	NAND gate	-2	1	*	*	UBL
SN74ALS00	NAND gate	-2	1	*	*	UBL
SN74LS241	Bus driver	-1~	1~	120	-150	UBL
SN74LS243	Bus driver	-1	1	120	-150	UBL
SN74LS245	Bus driver	-2	1	120	-150	UBL
SN74LS373	Register	-2/-0.1~	1/1~	120	-130	UBL
SN74LS641-1	Bus driver	-2	1	240	-150	UBL
SN74LS645-1	Bus driver	-2	1	240	-150	UBL
SN74S37	High performance driver	*	*	300	5	UBL

~ 3-state mode * not usable in this mode

Table 2-5 Examples of Standardised E-BUS Signal Loadings

2.5.3 LINE LENGTHS AND TERMINATING RESISTORS

The maximum permissible line length (11) of an E-BUS signal line is 500mm and corresponds to the length of a 19" rack. On E-BUS, signal line lengths between driver and E-Bus signal line should typically be 20mm. A length of 50mm must in no case be exceeded (see Fig. 2-15). Exceptions are possible on non-critical lines such as PRES-, NMI-, IORST- or analogue supply lines.

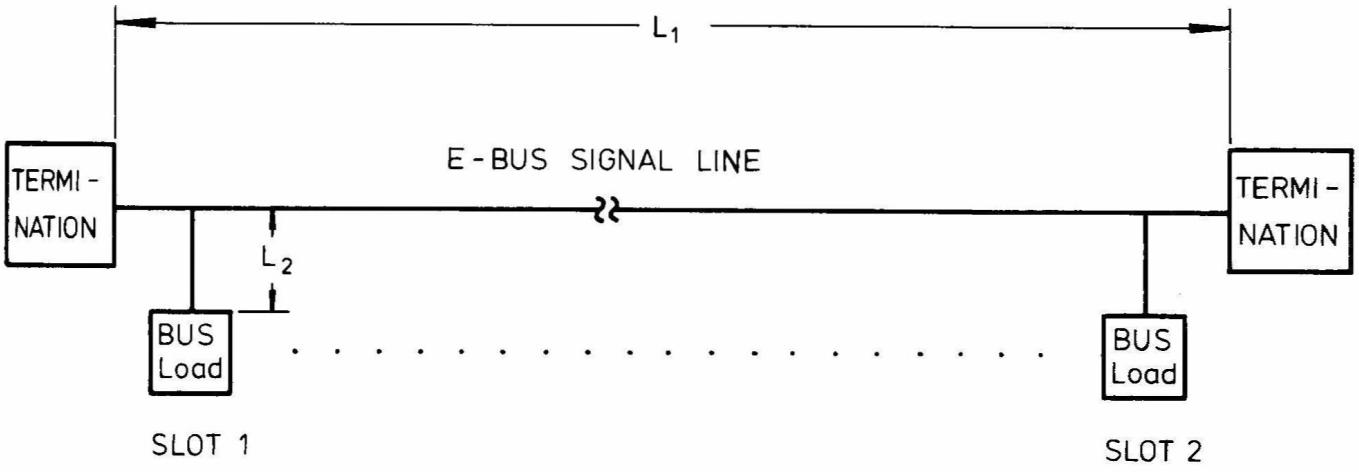


Figure 2-15 E-BUS Signal Line

The recommended card spacing is 4TE = 20.32mm (1TE = 5.08mm). The inductive and capacitive loading on a signal line should be less than 10uH and typically 10pF. The absolute limit per module is 20pF where the total capacitive load, distributed along the line, is not greater than 300pF. It should be noted that, on a module, no more than two 3-state drivers per signal line can be used since only 10pF is allowed for the output capacitance of each driver. The ohmic signal line resistance measured between pins in any two slots must be less than 1 ohm.

The line impedance of an E-BUS signal line must be 120 +/- 10 ohms. To avoid line reflections and to maintain valid logic levels when a line is not in use, line termination resistors are provided.

To maintain cost effectiveness between small and large E-systems it is necessary to differentiate between:

- MC (microcomputer) systems with BUSCLK-frequencies up to 3MHZ and 12 slots and
- MMC (multi-microcomputer) systems with BUSCLK-frequencies up to 10MHz and 21 slots

MC-Systems:

In microcomputer systems with BUSCLK- frequencies equal to or less than 3MHz, single ended line termination of the ADI bus and the control lines is sufficient (see Fig. 2-16). The right-most slot is always assigned to the MC-module. Where possible, single ended termination should be provided at a point on the signal line which is farthest away from the transmitting driver. A voltage divider (R1=390,R2=560) is used as line termination between Vcc, signal lines and ground except for the lines PRES-, NMI-, PWRFAIL-, IORST- and CRUIN which have a 1k ohm pull up resistor to Vcc.

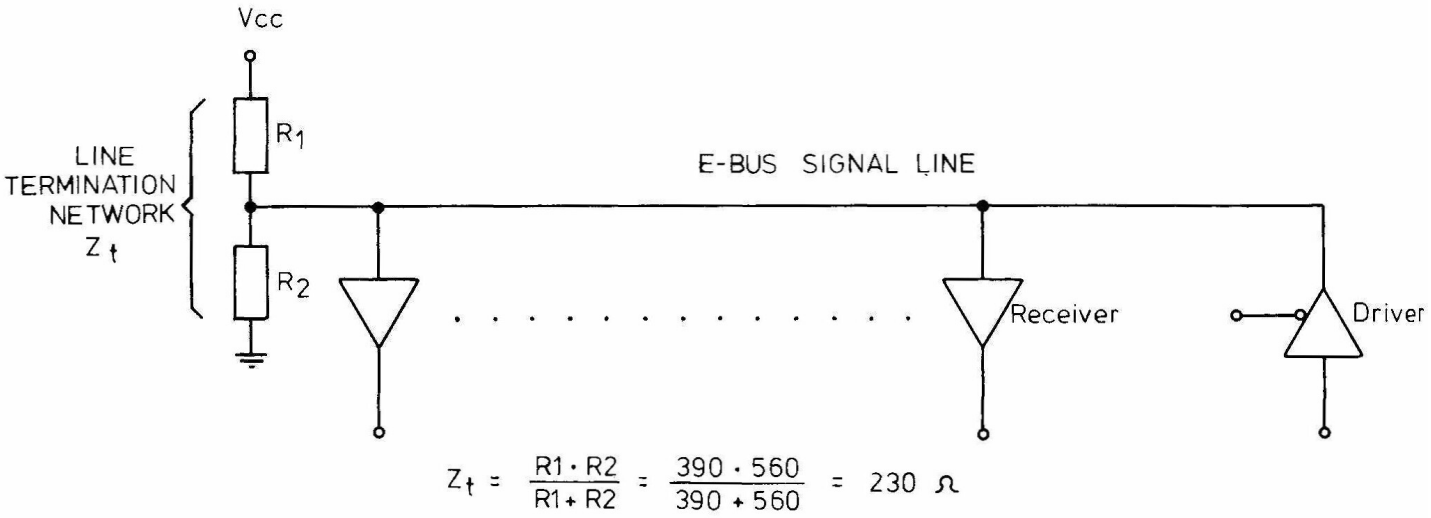


Figure 2-16 Single Ended E-BUS Termination in MC-Systems

The LOW level load (in UBLs) on a signal driver presented by the single ended line termination is as follows:

$$UBLt1 = \left(- \frac{Vcc - Vol}{R1} + \frac{Vol}{R2}\right) / 0.2 \text{ mA} \quad (1)$$

$$UBLt1max = \left(- \frac{Vccmax - Vol}{R1} + \frac{Vol}{R2max}\right) / 0.2 \text{ mA} = -63UBLs \quad (2)$$

The minimum HIGH level, Vth, produced by the terminating resistors (off load) is given by the following formula:

$$Vthmin = \frac{Vccmin}{R1max + R2min} \times R2min = \frac{4.85V}{429 \text{ ohm} + 504 \text{ ohm}} \times 504 \text{ ohm}$$

Vthmin = 2.62V (R1/R2 +/-10% tolerance)

The maximum HIGH level of Vth in the unloaded state is:

$$Vthmax = \frac{Vccmax}{R1min + R2max} \times R2max = \frac{5.15V}{351\ ohm + 616\ ohm} \times 616\ ohm$$

$$Vthmax = 3.28V$$

If at the HIGH level Voh < Vth, then the line termination supplies UBLs, however if Voh > Vth, then a loading in UBLs is produced .

The formula for calculating the UBLs in the HIGH state stems from a specific Voh level (usually 2.4V). The UBLs supplied or used are then calculated as follows:

$$UBLth = \left(- \frac{Vcc - Voh}{R1} + \frac{Voh}{R2}\right) / 0.02\ mA \qquad (3)$$

worst case conditions:

$$UBLthmin = \left(- \frac{Vccmin - Voh}{R1max} + \frac{Voh}{R2min}\right) / 0.02\ mA \qquad (4)$$

$$UBLthmin = -47UBLS \qquad Voh = 2.40V$$

This means that when Voh = 2.4V, the line termination supplies 47 UBLs with the worst case conditions given (Vccmin, R2min and R1max). The opposite worst case condition exists when Vcc = 5.15V, R2 = 560 ohms + 10% and R1 = 390 ohms - 10%.

$$UBLthmax = \left(- \frac{Vccmax - Voh}{R1min} + \frac{Voh}{R2max}\right) / 0.02\ mA \qquad (5)$$

$$UBLthmax = - 197\ UBLs$$

Since UBLthmin is then the lower value, limit calculations for the UBLs available at the HIGH level must assume this value. For example if a SN74LS241 is used as a driver on E-BUS, then the following minimum UBLs are available for modules on the bus:

LOW level:

$$UBLsink1 + UBLt1 + UBLs1 => 0 \qquad (6)$$

$$UBLsink1 = - UBLt1 - UBLs1$$

$$UBLsink1 = 63 - \frac{24\ mA}{0.2mA} = -57\ UBLs \quad (Vol = 0.5V)$$

HIGH level:

$$UBLsinkh + UBLth + UBLsh = < 0 \qquad (7)$$

$$UBLsinkh = -UBLth - UBLsh$$

$$UBLsinkh = 47 - \frac{-3\ mA}{0.02\ mA} = 197\ UBLs\ (Voh = 2.4V)$$

WARNING

Loading UBLs have a positive sign at the HIGH level and a negative sign at the LOW level. Therefore the total of all UBLs in the HIGH state must be less than or equal to 0, while at the LOW state the total must be equal to or greater than 0.

The 1k ohm (+/-10%) resistor to Vcc on the PRES-, NMI-, PWRFAIL-, IORST- and CRUIN lines supplies -111 UBLs in the HIGH state (Voh = 2.4V) and produces a load in the LOW state of -26UBLS (Vol = 0.5V).

For small E-BUS MC systems having less than 12 slots (@ 4 TE) and a BUSCLK- frequency of less then or equal to 3MHz, the single ended termination can be neglected.

MMC-Systems:

For MMC-systems with BUSCLK- frequencies up to 10MHz, the ADI bus and all control lines need double ended resistive termination networks (see Fig. 2-17). The double ended termination is also required for single processor systems having a BUSCLK- frequency greater than 3MHz.

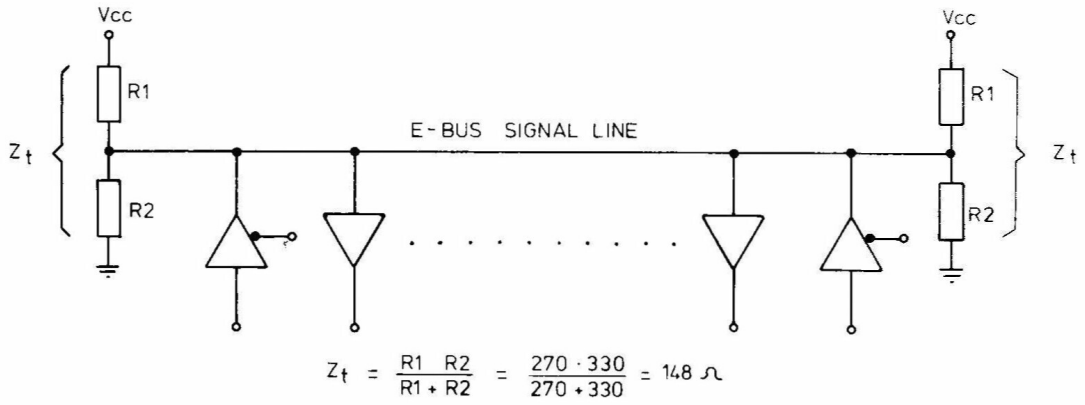


Figure 2-17 Double Ended E-BUS Termination in MMC-systems

The value of R1 is 270 ohms (+/-2%) and for R2 is 330 ohms (+/-2%). For a complete E-BUS chassis (21 modules with about 10pf/module) a nominal impedance of about 50 ohms should be assumed. The reflection factor is:

$$R = \frac{Zt - Zo}{Zt + Zo} = \frac{148 - 50}{148 + 50} = 0.495$$

and is thus under the permitted 0.5 limit. The minimum HIGH level Vth (no load) is calculated by formula 2:

$$Vthmin = \frac{4.85V}{275.4\ ohm + 323.4\ ohm} \times 323.4 = 2.62V$$

Half the loading at the LOW level is as given in formula (1):

$$UBLt1 = \left(- \frac{5.15V - 0.5V}{275.4\ ohm} + \frac{0.5V}{323.5\ ohm}\right) / 0.2\ mA = -80\ UBLs$$

Thus at the LOW level the line termination loads the driver with 2 x (-80) = -160 UBLs.

Half the loading at the HIGH level is as given in formula (4):

$$UBLth = \left(\frac{4.85V - 2.4V}{275.4\ ohm} + \frac{2.4V}{323.4}\right) / 0.02\ mA = -73\ UBLs$$

Thus at the HIGH level for Voh = 2.4V the double ended termination supplies 2 x (-73) = -146 UBLs. If drivers with open outputs are used (e.g. for BUSY-) then for 21 modules the HIGH level can be loaded with an average of 3.8 UBLs. With active drivers (e.g. SN74LS641-1) another -150 UBLs (Voh = 2.4V) are available in the HIGH level.

Signal drivers for E-BUS lines with double ended termination must be able to drive a minimum of Iol = 48mA at the LOW level (where Vol = 0.5V). For example, if the SN74LS641-1NL is used, then the following minimum UBLs are available for other modules on the E-BUS:

LOW level:

$$UBLsink = -2UBLtl - UBLsl$$

$$UBLsinkl = 160 - \frac{48\ mA}{0.2mA} = -80\ UBLs \quad (Vol = 0.5V)$$

HIGH level:

$$UBLsinkh = -2UBLth - UBLsh$$

$$UBLsinkh = 146 - \frac{-3mA}{0.02mA} = 296\ UBLs\ (Voh = 2.4V)$$

WARNING

Loading UBLs have a positive sign at the HIGH level and a negative sign at the LOW level. The sum of all UBLs must therefore be equal to or less than 0 in the HIGH state, and equal to or greater than 0 in the LOW state.

Fig. 2-18 shows the recommended value and location of the line termination for all E-BUS signal lines.

Backpanel line termination				
E-Bus signal	Single Processor systems		Multiprocessor systems	
	Left Slot*	Right Slot	Left Slot*	Right Slot
A0/D0/INT0- A6/D6/INT6	390/560´	-	270/330+	270/330
A7/D7- A15/D15/CRUOUT	390/560	-	270/330	270/330
XA0 - XA3	390/560	-	270/330	270/330
INTEN-	-	390/560	270/330	270/330
ALATCH-	390/560	-	270/330	270/330
MEMEN-	390/560	-	270/330	270/330
DEN-	390/560	-	270/330	270/330
WE-	390/560	-	270/330	270/330
BUSY-	-	390/560	270/330	270/330
READY-	-	390/560	270/330	270/330
AREADY-	-	390/560	270/330	270/330
MEMWIDTH	390/560	-	270/330	270/330
BUSCLK-	390/560	-	270/330	270/330
PRES-	-	1k Pull up	-	1k Pull up
IORST-	1k Pull up	-	1k Pull up	-
NMI-	-	1k Pull up	-	1k Pull up
PWRFAIL-	-	1k Pull up	-	1k Pull up
GRANTIN	-	-	-	-
GRANTOUT	-	-	-	-
CRUIN	-	1k Pull up	-	1k Pull up
CRUCLK-	390/560	-	270/330	270/330

all values in Ohms * front view ´ +/-10% + +/-2%

Figure 2-18 E-BUS Signal Line Termination

2.5.4 BACK PLANE CHARACTERISTICS

An E-system back plane must correspond to the technical data given in table 2-6. For small systems with 2-12 slots, a double sided board is sufficient, while for BUSCLK-frequencies greater than 3MHz and 2-21 slots a minimum of four layers must be used (one Vcc and one Gnd).

The following is recommended:

- as far as possible, place terminating resistors on the back plane board.
- GRANTIN/GRANTOUT jumpers to be provided per slot.
- ANACOM-GND jumper provided if necessary.
- connect all the 64 pins of the DIN 41612 (form C) connector in parallel, including reserved signal lines. Provision for termination resistors should also be made on reserved lines.
- clamp, screw or pin connections for all supply voltages, PWRFAIL-, PRES-, NMI- and +5Vstby to be provided on reverse side (minimum of 2 x GND and 2 x Vcc). A sense connection should also be provided for +5V.
- a bus timeout counter should be provided to prevent system stop if a memory instruction accesses a non-existent memory location, by activating READY-/AREADY-. See section 4.4 and the E5000 Backplane Users Manual.

	Min.	Typ.	Max.	
- signal line impedance	110	120	130	ohm
- bus line length			500	mm
- signal conductor width		0.25	0.3	mm
- signal conductor resistance		0.8	1.0	ohm
- board thickness per layer			1.6	mm
- number of layers				
. 2-12 slot (3MHz)	2			layers
. 12-21 slot (3-10MHz)	4			layers
- copper thickness	35	70		um
- resistance				
. +5V,GND			10	mohm
. +12V,-12V,+15V -15V,+5VSTBY,ANACOM and +BATT			100	mohm
- slot interval	3	4		TE*

* 1TE = 2.08mm

Table 2-6 E-BUS Back Plane Technical Data

2.5.5 SIGNAL DRIVER AND RECEIVER

It is recommended that devices from the LS and ALS TTL series are used for E-BUS signal drivers and receivers. Electrical parameters for various types of E-BUS drivers for MC and MMC systems are summarised in Fig. 2-19.

Signal line	Driver type*	MC-Systems		MMC-Systems	
		Iol	Ioh	Iol	Ioh
A0/D0/INT0 - A6/D6/INT6, A7/D7 - A15/D15/CRUOUT, XA0 - XA3, MEMEN-, WE-, MEMWIDTH, ALATCH, CRUCLK-, DEN-	3-State-output	24mA Vol= 0.5V	-3mA Voh= 2.4V	48mA Vol= 0.5V	-3mA Voh= 2.4V
READY-, AREADY-,BUSY-	Open collector output	24mA Vol= 0.5V	0.1mA Voh= 2.4V	48mA Vol= 0.5V	0.1mA Voh= 2.4V
PRES-, IORST-, NMI-, PWRFAIL-, CRUIN	Open collector output	16mA Vol= 0.5V	0.1mA Voh= 2.4V	16mA Vol= 0.5V	0.1mA Voh= 2.4V
INTEN-	Open collector or 3-state output	24mA Vol= 0.5V	-3mA/ 0.1mA Voh= 2.4V	48mA Vol= 0.5V	-3mA/ 0.1mA Voh= 2.4V
BUSCLK-	3-State or Totem-Pole-output	24mA Vol= 0.5V	-3mA Voh= 2.4V	48mA Vol= 0.5V	-3mA Voh= 2.4V
GRANTOUT	Open collector output	8mA Vol= 0.5V	0.1mA Voh= 2.4V	8mA Vol= 0.5V	0.1mA Voh= 2.4V

* Cout = <10pF

Figure 2-19 Signal Driver Type and Capability for MC and MMC systems

The following devices are recommended as preferred types:

	MC Systems	MMC Systems
3-state output	SN74LS24XNL	SN74LS64X-1NL
Open collector output	SN74LS38NL	SN74S38NL
Totem pole output	SN74LS37NL	SN74S37NL

For E-BUS signal receivers all the normal LS and ALS TTL devices having a loading of 1 or 2 UBLs per input are suitable.

Devices having Schmitt-Trigger inputs are especially recommended for use with control lines (e.g. SN74LS24X). This is particularly true for ALATCH.

The use of STTL drivers should be avoided to minimise cross talk except where the necessary speed or drive capability is not available from a device in the LS or ALS series.

2.5.6 VERIFICATION OF SIGNAL AND SUPPLY LOADING

In an E-system with a given complement of modules the signal loading on each signal line should be checked. Fig. 2-20 shows a form to aid signal loading monitoring during development of new E-BUS modules. The average signal loading should be 2 UBLs (LOW and HIGH). Using the signal loading figures for standard or self developed E-BUS modules the signal loading within the complete system can be computed. Fig. 2-21 shows a table to assist with the determination of total loading per signal or signal group. This table must be verified for both HIGH and LOW levels separately.

The sum, including loading by the line termination (UBLterm, first column in Fig. 2-21), must be equal to or greater than 0 for the LOW level and equal to or less than 0 for the HIGH level (negative UBLs). The form shown in Fig. 2-22 may be used to calculate the loading on the supply, which may include a battery supply. As well as the type of E-BUS module used, the position of the GRANTIN/OUT jumpers should also be considered.

TM990/E-Module:					
E-Bus Signal	IN/ OUT	Driving UBL's		Consuming UBL'S	
		LOW	HIGH	LOW	HIGH
A0/D0/INT0- A6/D6/INT6, A7/D7					
A8/D8- A15/D15/CRUOUT					
XA0 - XA3					
INTEN-					
ALATCH-					
MEMEN-					
DEN-					
WE-					
BUSY-					
READY-					
AREADY-					
MEMWIDTH					
BUSCLK-					
PRES-					
IORST-					
NMI-					
PWRFAIL-					
GRANTIN					
GRANTOUT					
CRUIN					
CRUCLK-					

1UBL (LOW) =0.2mA; 1UBL (HIGH) = 0.02mA

Figure 2-20 E-BUS-module UBL table

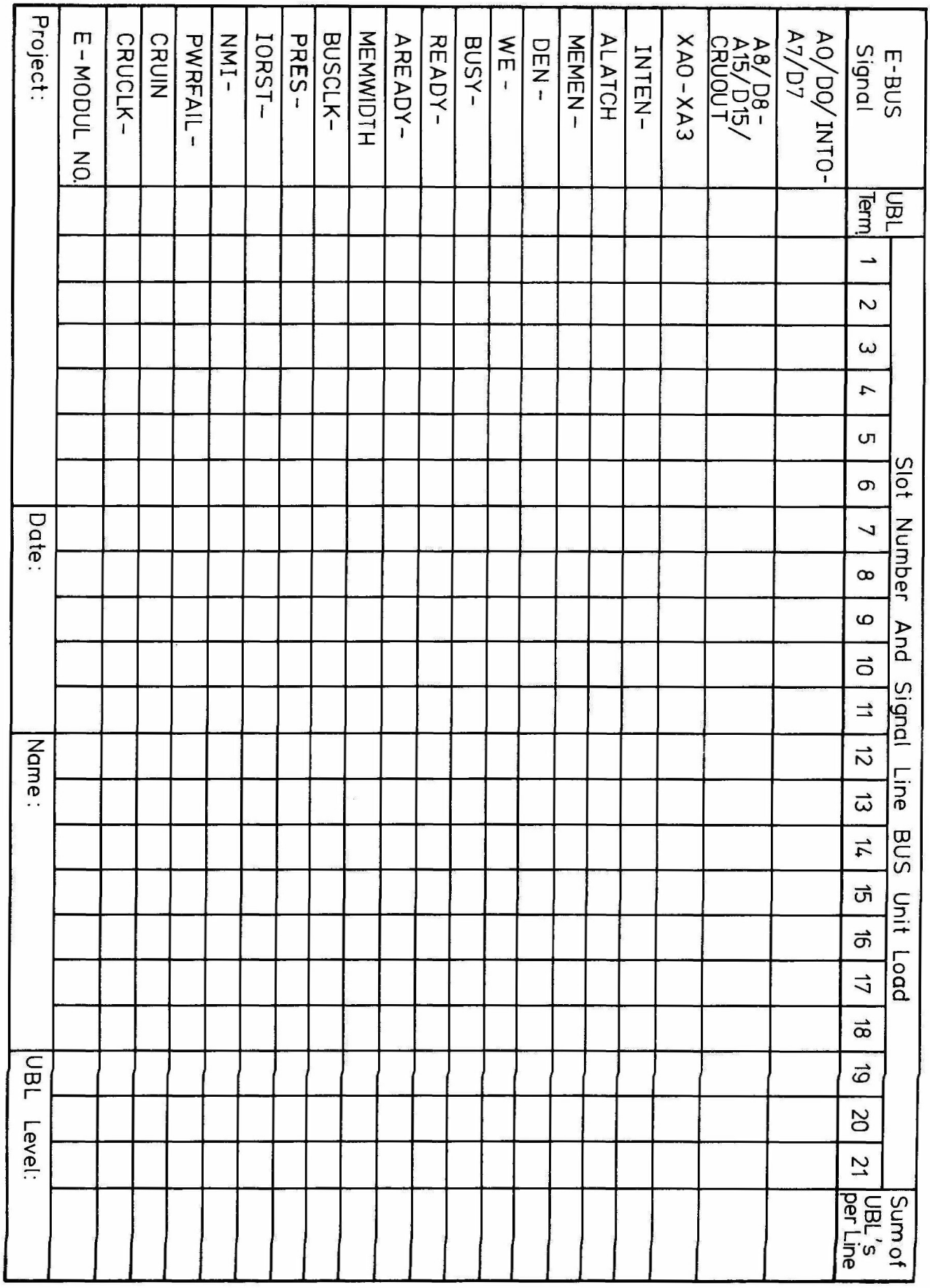


Figure 2-21 E-Systems UBL Loading Table

E-BUS voltage supply	Slot Number And Maximum Current Per Module																					Totals	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	I[A]	P[W]
+5V																							
+5V STBY																							
+BATT																							
+12V																							
+15V																							
-12V																							
-15V																							
Grantin to Grantout Jumper																							
MMC-Module																							
DMA-Module																							
Interrupt-XMT																							
Interrupt-Receive																							
Module Type																							
Project :							Date:						Name:						PW$_{max}$:				

SECTION 3

MULTI-MICROCOMPUTER SYSTEMS

The following chapter describes possible realisations of multi- microcomputer systems (MMC Systems) based on the E-BUS. These are general guidelines which simplify the independent generation of such systems now using special hardware and software. The basic structures for bus coupling, priority control and types of input/output are discussed.

3.1 SYSTEM STRUCTURES

In an E-system there are principally three different system structures:

1. Single microcomputer system (Single Master System).
2. Multi-microcomputer system (Multi Master System).
3. Decentralised multi-microcomputer system (Distributed Multi Master System).

The type of bus coupling used is an important distinguishing feature between the different system structures. E-BUS supports two forms of bus coupling:

- tight bus coupling
- loose bus coupling

An E-system can contain up to 8 tightly coupled multi-microcomputer modules each having a maximum of 16 interrupt levels. It is also possible to allow a larger number of MMC-modules with a different division of the 128 interrupt levels available.

The only limits to the number of tightly coupled modules on E-BUS are the available number of slots and time constraints. This is also true for loosely coupled modules.

3.1.1 TIGHT BUS COUPLING

It is control of the bus which produces the concept of tight bus coupling on E-BUS. Each master module is allowed complete control over E-BUS and all connected slave modules, subject to their assigned priorities. The block diagram in fig.3-1 shows a multi-microcomputer system using tight bus coupling. The memory and input/output modules connected to E-BUS can be mapped within the address range so as to produce either common or private resources.

The particular requirements of the system dictate the arrangement of common and private modules.

To minimise the necessary software overhead it is recommended that common memory or I/O ranges are only used for planned redundancy (e.g. supervision module) and/or to facilitate communication between MMC modules.

The control of common input/output modules is further explained in section 3.5.3.

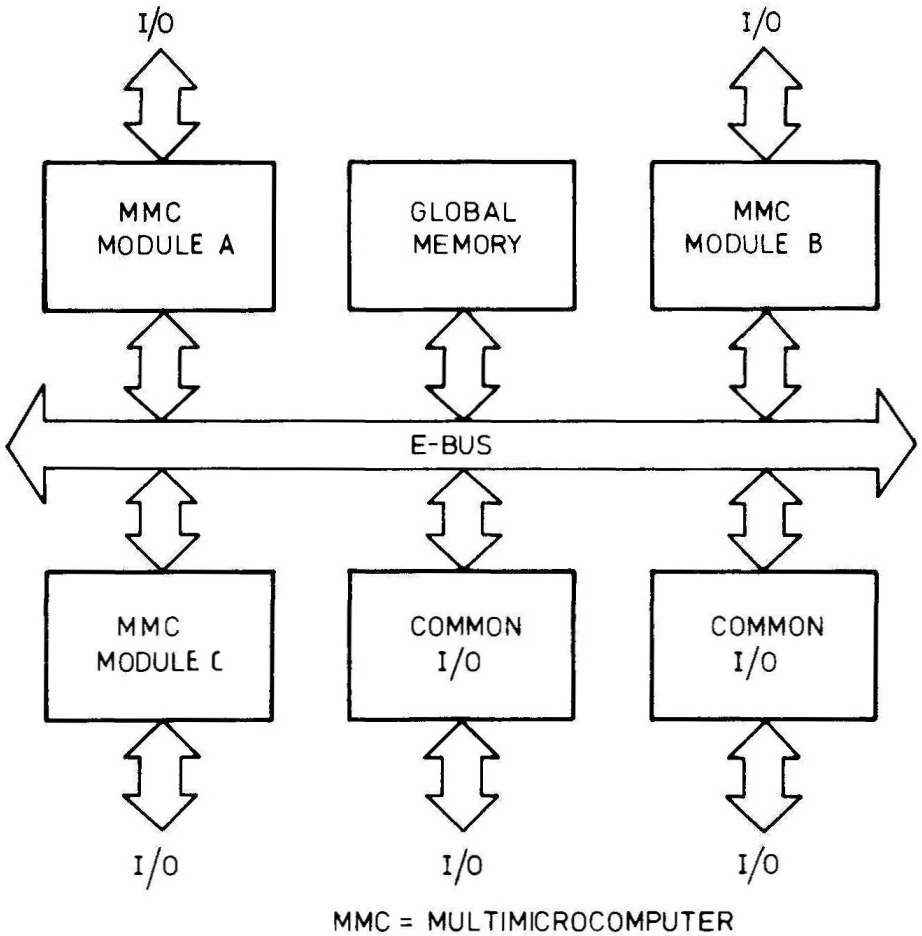


Figure 3-1 Multi-Microcomputer with Tight Bus Coupling

A block circuit diagram of an MMC-module is shown in fig.3-2. As well as having input/output each MMC-module should have as much local program and data memory as possible in order to keep the number of bus arbitrations necessary as low as possible. The number of tightly coupled MMC-modules is limited by time constraints on E-BUS. Fig.3-3 shows that the average degree of E-BUS use per module is dependent on the number of MMC-modules on the bus. It is recommended that the combined usage of all bus controllers (MMC-modules and DMA modules) should not exceed 80% of total bus time, since reserves must be available for interrupt transmission, bus control and synchronisation. A module's bus usage is the sum of the times the bus is used by the module, as a percentage of total time. As an example, a DMA module that requires the bus for 270us every 5ms imposes a 5.4% bus load.

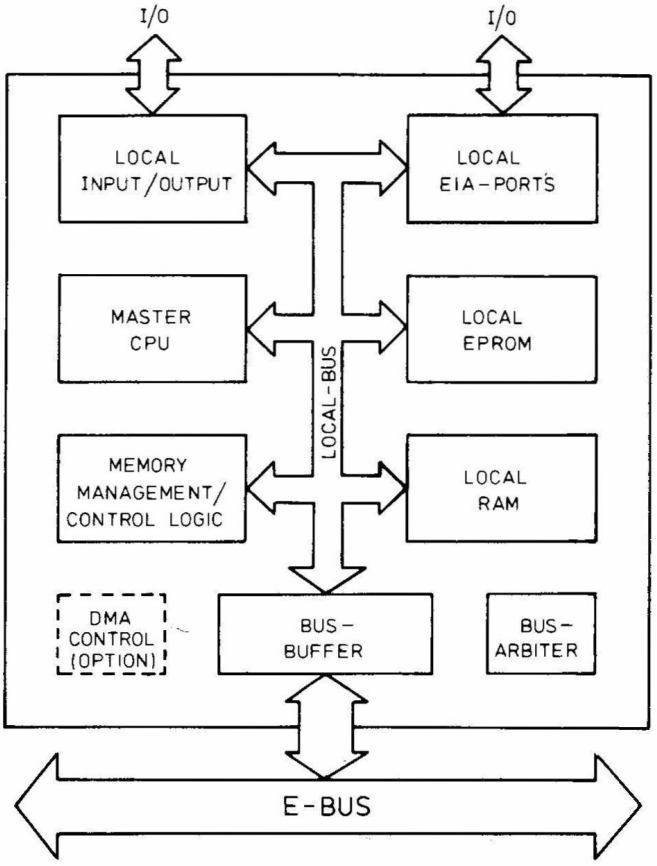


Figure 3-2 Block Circuit Diagram of an E-BUS Multi-Microcomputer

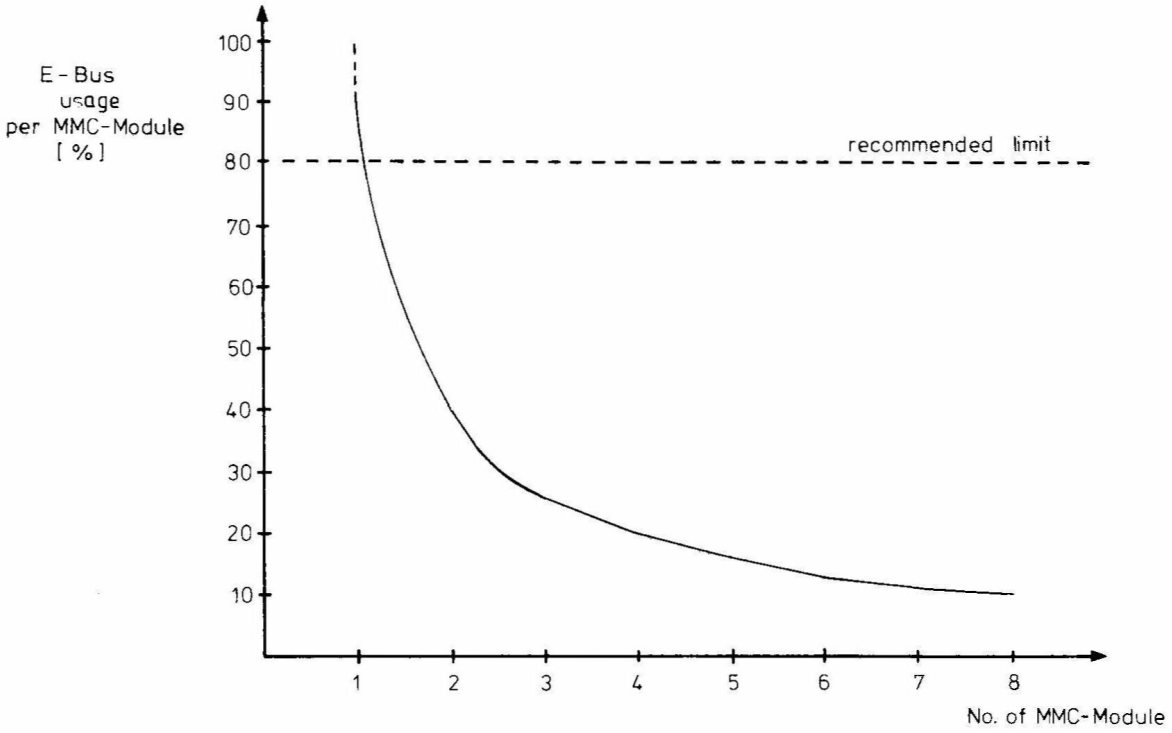


Figure 3-3 Dependence of E-BUS Use on Number of MMC Modules

An MMC-module contains bus control (bus arbiter), memory management (e.g. SN74LS610 memory mapper) and control logic as well as the microprocessor. If the EPROM/RAM on the module is to be common memory, or if it is to be accessible by an external peripheral control unit (e.g. floppy disc control) then a DMA controller or a dual port RAM must also be provided. If the MMC-module does not have control over E-BUS and the address of the local memory is selected then the DMA controller must switch the MMC-module into operation as a memory module, during which time the microprocessor is in the hold state.

3.1.2 LOOSE BUS COUPLING

Loose bus coupling on E-BUS means that a module or E-system (e.g. intelligent control unit) cannot assert direct control over the bus. The exchange of data and commands then occurs either via a

- dual access memory (DPM = Dual Port Memory) or
- the input/output interface

The dual port memory must be functionally arranged such that it can be written to and read from both sides. This means that the two memory ports must be within the address ranges of the two microcomputer systems (see example in fig.3-4).

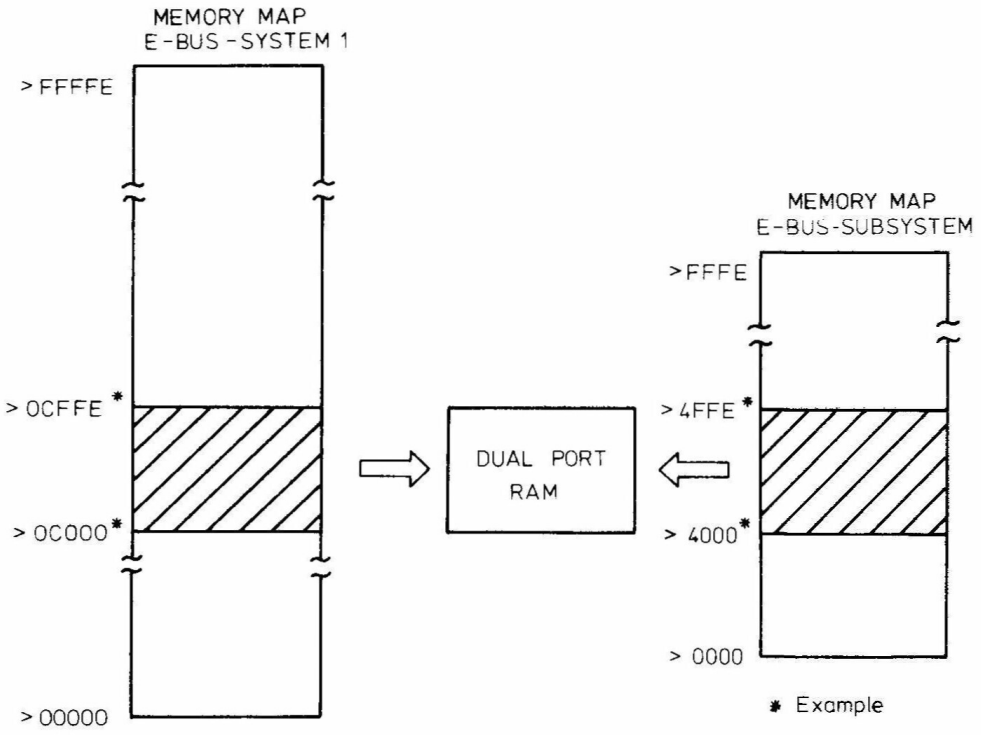


Figure 3-4 Memory Maps for Loose Bus Coupling Via Dual Port Memory

Indirect coupling of two E-BUS systems or between one E-BUS and the local bus of an intelligent control unit can be provided using a DPM.

Fig.3-5 shows two E-systems linked via loose bus coupling. Both systems are completely autonomous and exchange data and commands via the dual port memory.

The compact nature of E-BUS enables this form of loose bus coupling to be realised very simply.

The use of a larger card format (e.g. 233mm x 160mm) with two 64 pin E-BUS connectors enables two E-systems each using single card format (160mm x 100mm) to be coupled.

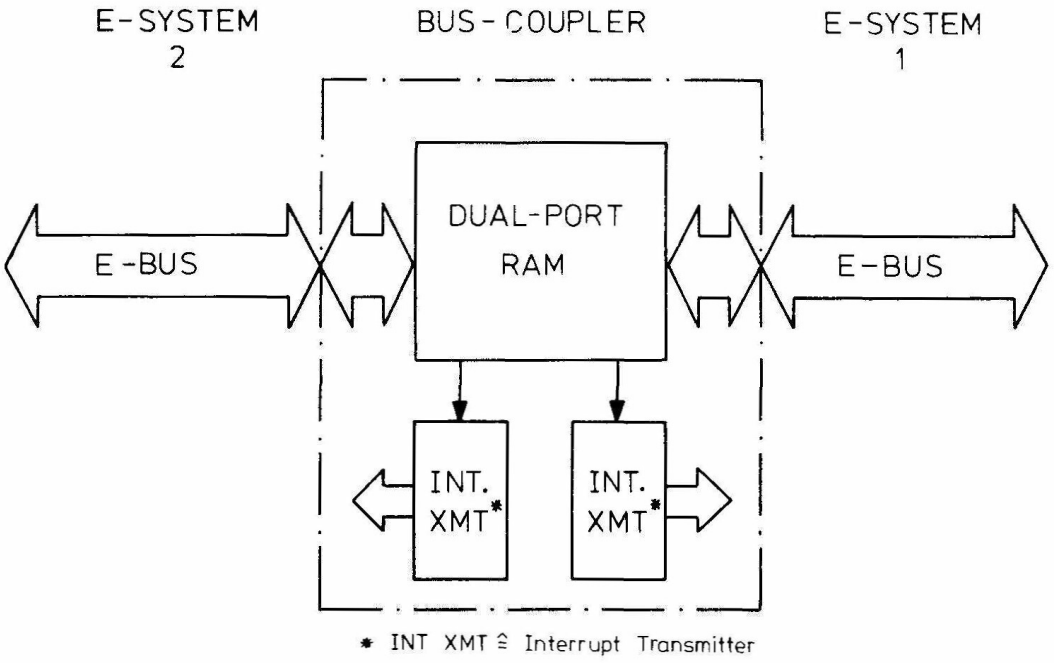


Figure 3-5 Loose Bus Coupling of Two E-Systems

If within an E-system loose bus coupling is required between E-BUS and the local microprocessor bus of an intelligent control unit, this can also be achieved using a dual port memory. Fig.3-6 shows a block diagram of loose bus coupling between an MMC-module on E-BUS and an intelligent control module. The intelligent control module provides memory and input/output via a local microprocessor. Optionally a DMA controller can be used, in a common memory range on E-BUS, for fast data transfer.

To simplify the exchange of data and commands it is recommended that two independently executing programs are synchronised using interrupts. An interrupt of the local microprocessor on the intelligent control unit can automatically be generated once the MC or MMC-module writes to a particular memory address in the dual port memory. The transmission of a complete interrupt code (MMC-module address and interrupt level) from the intelligent control to an MC or MMC E-BUS module should be software programmable (see section 7.3.1).

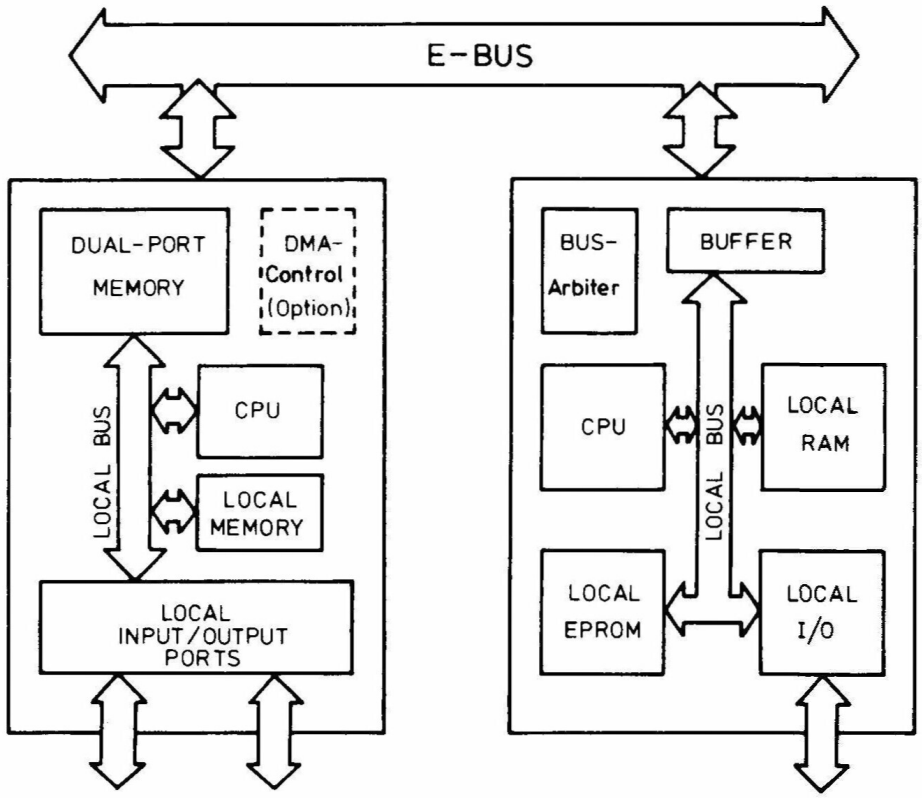


Figure 3-6 Loose Bus Coupling between E-BUS and a Local Bus

Loose bus coupling between E-systems or MC-modules and intelligent control units can be realised using the input/output interface in a similar manner to coupling using a dual port memory. A dual access input/output port is produced which is analogous to the dual port memory. The advantage of using dual access input/output ports for loose bus coupling lies in the low cost incurred. A disadvantage is that data exchange can only occur serially in byte or word transfers whereas with dual port memories complete data blocks can be sequentially transferred. This often results in minimal software and time overhead for the controlling microprocessor.

The various means for loose bus coupling described so far assume that the signal line length between devices is very short. To couple E- systems over greater distances it is possible to resort to other byte or bit serial interfaces (see fig.3-7). The type of transmission system can be any of the following (see also fig.3-8):

- bidirectional transmission line (party line)
- unidirectional point to point connection
- bidirectional ring line

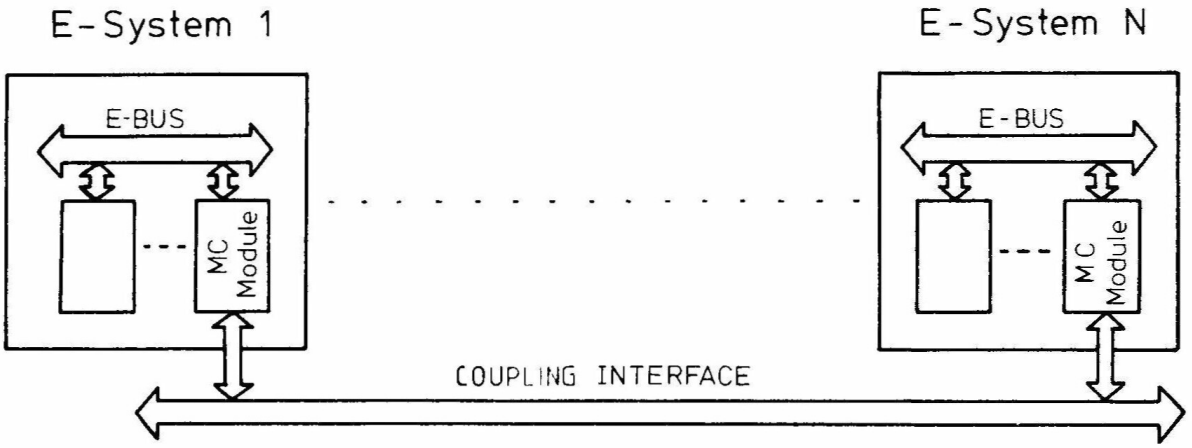


Figure 3-7 Coupling of Decentralised E-Systems

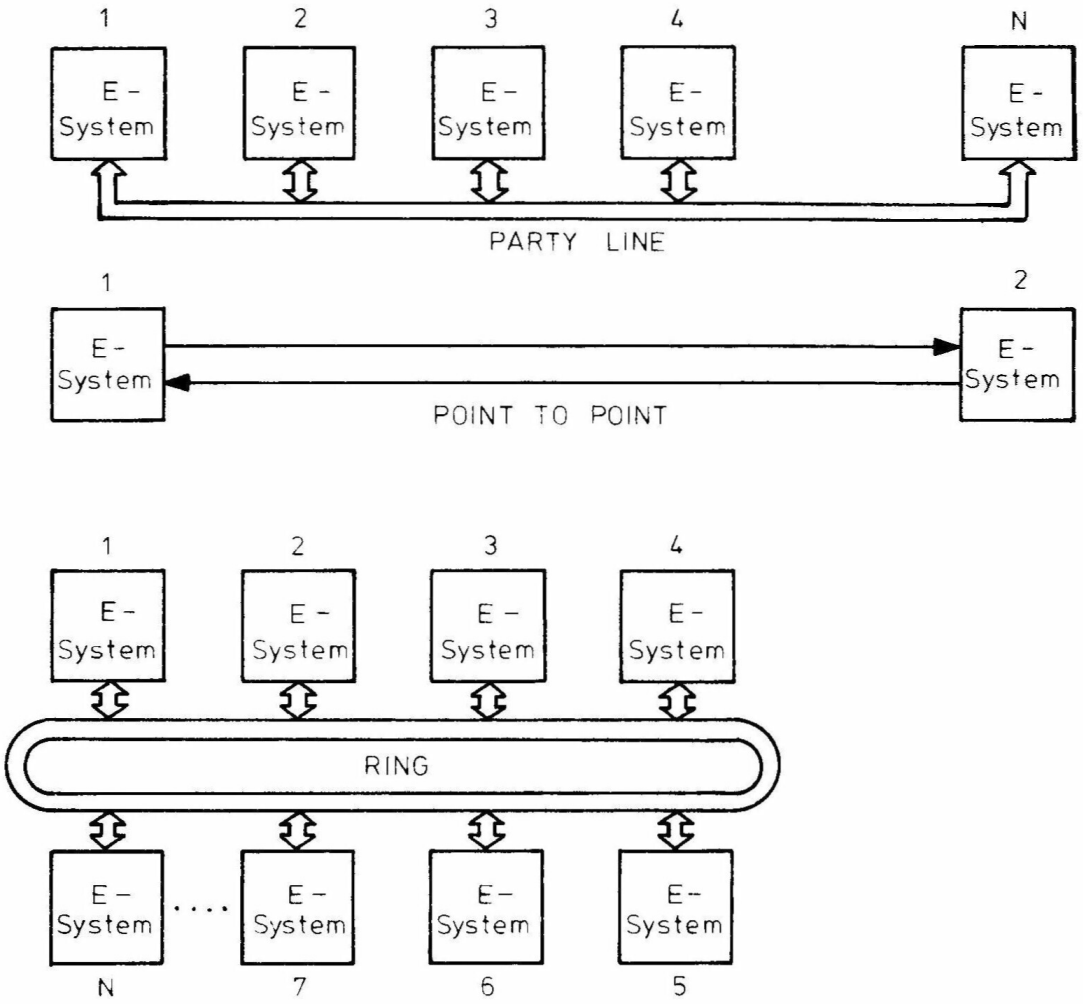


Figure 3-8 Types of Transmission System for Coupling Decentralised E-Systems

The interface to be used can be chosen from consideration of the resultant cost, transmission speed, distance, noise immunity and software overhead. Table 3-1 shows important selection criteria for the different interfaces which are supported by E-Systems. In industrial applications with enforced separation the party line concept has been developed by Texas Instruments and is characterised by a high level of noise immunity. The synchronous HDLC package (High Level Data Link Control) is a software package which is available for control of this interface. It provides exchange of data and programs between a primary and up to 32 secondary stations (master slave configuration).

Coupling	IEC Bus	RS232C	RS449 Asynch.	RS449 Synch.	TI Industrial Protocol	RS232 & Modem
Party Line						
Point to Point						
Ring Line						

Interface	Transmission Format	Transmission Rate	Max. Distance	Elect. Isolated	Protocol
IEC Bus	Byte serial	<250kB	20m	-	IEEE
*RS232C	Serial	<76kB	100m	-	EIA
*RS449 Asynch.	Serial	<500kB	1000m	-	EIA
*RS449 Synch.	Serial	<1MB	2000m	-	EIA
TI Party Line	Serial	<9.6kB	1000m	Yes	HDLC
*RS232C & Modem	Serial	<9.6kB	some km	Yes	EIA

Table 3-1 Interfaces for Coupling Decentralised E-Systems

3.2 PRIORITY ASSIGNMENT

Tightly coupled MMC-modules on E-BUS are assigned priorities for bus arbitration either by the serial daisy chain or via a parallel priority controller. The type of modules requiring bus arbitration may be autonomous multi-microcomputer, DMA or input/output modules with interrupt sources.

The assignment of a priority to a module must comprehend the following aspects:

- max. permissible reaction time
- average usage of E-BUS by the module

Priority control by means of the serial daisy chain is the most cost effective method and the use of parallel priority control is only required if:

- the time delay of the serial daisy chain is too great to determine priority within one BUSCLK- cycle

- the max. possible reaction time through the hierarchical arrangement of priorities is too great

3.2.1 SERIAL DAISY CHAIN

Assuming that within a 19" chassis a maximum of 21 modules can be connected to E-BUS (card interval = 4TE) then the maximum BUSCLK- frequency can be deduced from the formula:

$$F_{max} = \frac{1}{tp + N \times tpg + tpg + tsb}$$

The propagation delay time (tp) is the maximum delay between the positive edge of BUSCLK- on a module asserting a bus request and it setting the GRANTOUT line. The time tpg is the propagation delay on a module required to feed the GRANTIN signal to GRANTOUT, while tsb is the set up time required by the bus controller (arbiter) on the GRANTIN line.

The relevant maximum times for MMC-systems with a BUSCLK-frequency up to 5 MHz are specified below:

tp=20ns, tpg=8ns and tsb=20ns

Thus from a given BUSCLK- frequency the maximum number of modules in series can be deduced. Fig.3-9 shows the dependence of the number of modules on the BUSCLK- frequency. It should be noted that modules having the GRANTIN/GRANTOUT lines shorted (e.g. memory modules) have no influence on the maximum number of modules in the daisy chain.

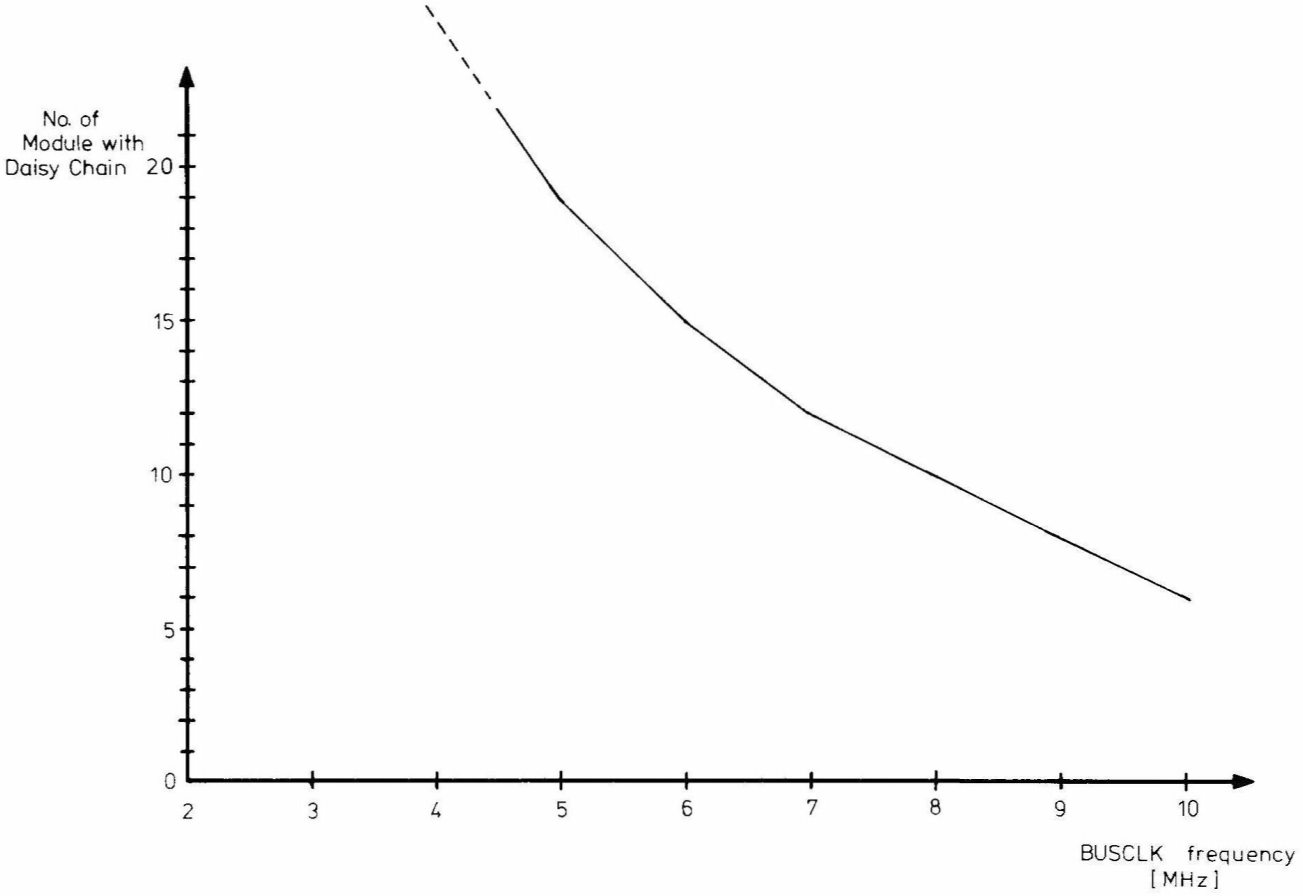


Figure 3-9 Number of Daisy Chain Modules on E-BUS

In order to select a slot for a module it is necessary to calculate the average E-BUS usage required by that module. Once the usage is known the following general rule is applicable:

- the priorities of modules on E-BUS should be in reverse relation to the bus loading of the modules (highest bus loading -- lowest priority, and lowest bus loading -- highest priority).

Accordingly interrupt modules are assigned the highest priority in the daisy chain (bus loading less than 2%), followed by DMA and MMC-modules. Within the chain the priority of the interrupt modules can be selected according to the priorities of the interrupts generated. With DMA and MMC-modules the priority should be assigned according to the bus occupation and the permissible delay time of a bus request. The maximum delay time of a module bus arbitration is computed from the total of the individual bus arbitrations

of modules with higher priority. In order to assign enough time for arbitration of the bus by MMC and other low priority modules it is necessary to organise the higher priority module bus arbitrations into time slots.

With input/output operations it is better to minimise the bus loading by using interrupts than to request I/O flags (polled I/O). If cyclic I/O flag requests cannot be avoided then the number of bus requests should be kept as low as possible. This may be realised simply by the use of wait loops or timer delays.

The software for a system of MMC-modules must be designed using a common set of rules. There is a choice between block oriented and single cycle access. In either case the time between bus accesses of one module must be long enough to allow other MMC-Modules to execute any necessary bus operations. If a block oriented access is chosen, the bus accesses of MMC-modules are synchronised automatically by the given priority in the daisy chain. The advantage of block oriented access is the minimal time lost in synchronisation. The disadvantage is that an MMC-module with a lower priority may have to wait longer before it can gain access to the bus.

3.2.2 PARALLEL PRIORITY CONTROL

E-BUS modules may utilise parallel priority control by using parallel access to the GRANTIN/GRANTOUT lines with a special back plane. Fig. 3-10 shows a block diagram of parallel priority bus control. The module bus requests (GRANTOUT) are fed in parallel to the bus control unit which is capable of freely assigning priorities. The priority arrangement can be produced in the following ways:

- time slot process with fixed sequence and occupation time for each module
- sequential arrangement in chronological sequence of bus requests
- dynamic priority assignment according to frequency of bus requests

Parallel priority control allows flexible control of bus arbitration corresponding to current system requirements. Apart from pure priority control the parallel bus control unit also offers the possibility of isolating a faulty module from E-BUS.

Bus operations can be supervised, and potential bus blocking (caused, for example, by one controller attempting to address non-existent memory - no READY- signal returned) can be

detected and properly handled. When using GRANTOUT for parallel control it should be remembered that GRANTIN and GRANTOUT are connected via an AND function to facilitate serial daisy chain control, thus to produce a valid bus request the GRANTIN input on the module must be HIGH or the module logic modified by using a jumper.

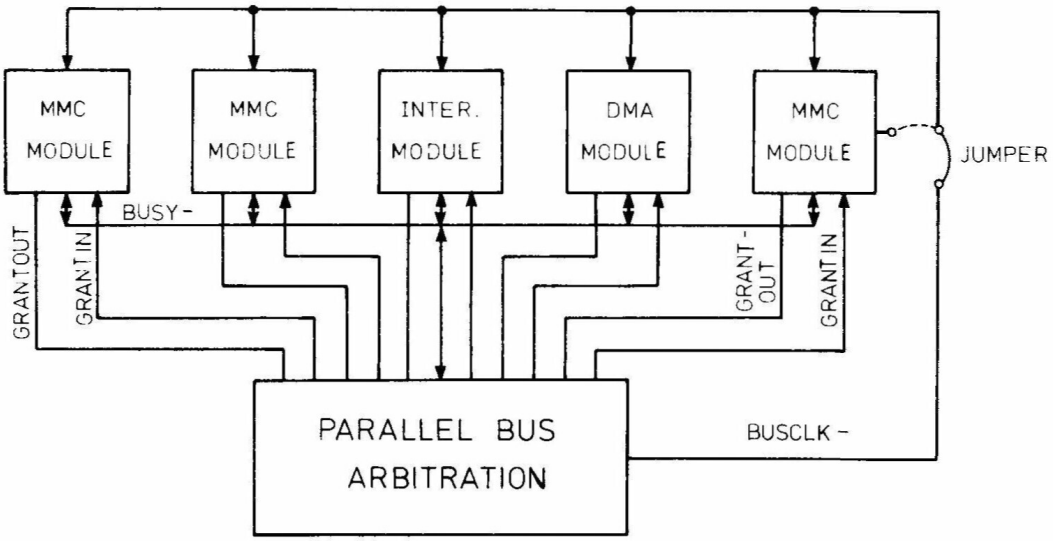


Figure 3-10 E-BUS Parallel Priority Control

Since module bus arbitrations are synchronised with the positive edge of BUSCLK- the parallel bus control can set GRANTIN HIGH during BUSCLK- HIGH. If the GRANTOUT line on the module is then LOW a bus request is present. On the negative BUSCLK- edge the bus control unit can then select the highest priority module and while BUSCLK- is LOW, enable a bus arbitration; GRANTOUT goes HIGH. Synchronisation of the module to E-BUS occurs as in section 2.3.2.2.

Fig.3-11 shows the timing diagram of parallel bus control for modules designed for serial daisy chain control. An alternative is to use a jumper on the module to select between serial and parallel bus control (see fig.3-12). Position S1 of the jumper is for serial and position S2 for parallel bus control. A mixture of serial and parallel control (e.g. several interrupt sources on one module) is allowable.

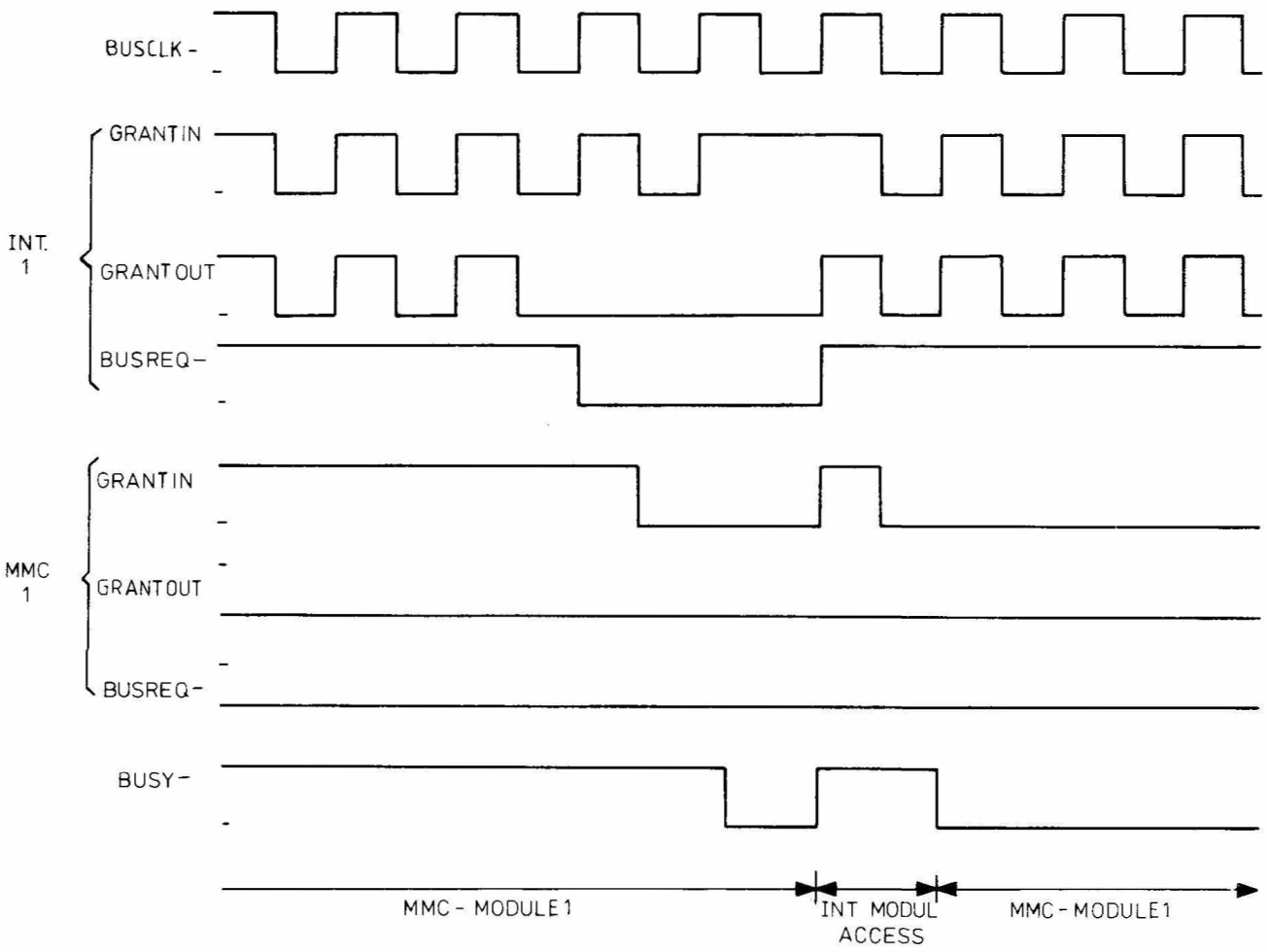


Figure 3-11 Timing Diagram for Parallel Priority Control

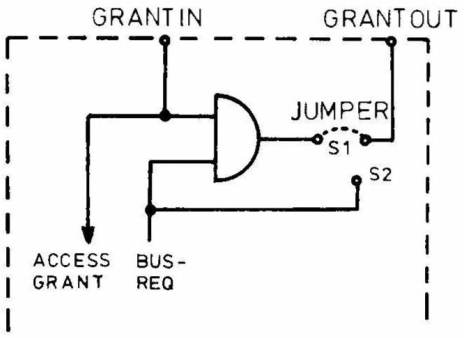


Figure 3-12 Selection of Parallel or Serial Priority Control

3.3 CLOCK GENERATION

In an E-system with several MMC-modules the BUSCLK- is generated by a single source. Although each MMC-module has its local clock source, BUSCLK- is either generated by one MMC-module or by a separate clock generator on one of the other modules. It must be possible to disconnect the BUSCLK- source on each MMC-module by use of a jumper (see fig.3-13). On an MMC-module the bus controller (bus arbiter) must control the synchronisation between the local clock and BUSCLK-. The necessary clock synchronisation is described in section 7.6.

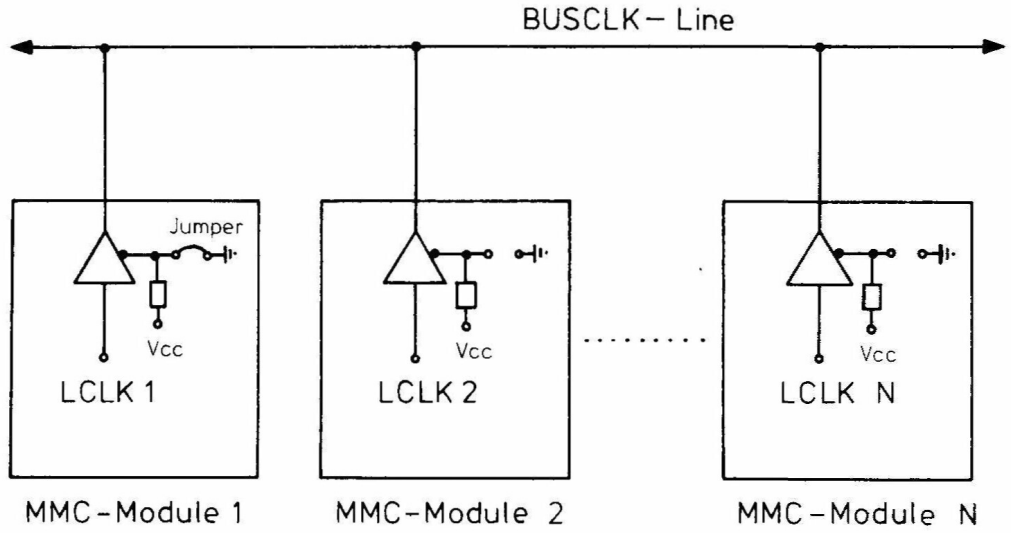


Figure 3-13 BUSCLK- Generation in Systems with Several MMC Modules

The bus operations are generated by the current bus master synchronously to its local clock. This means that normally bus operations of only one bus master are synchronous with BUSCLK- (MMC-module 1 in the example of fig. 3-13). Hence modules in MMC-systems must be able to operate asynchronous to BUSCLK-. This requirement does not create problems on fast modules, as the READY- signal can then be driven directly from the address decoder logic. On slow modules, the generation of wait cycles can be accomplished by either delay lines or a counter. If the delay times for READY- are generated by a BUSCLK- counter, synchronisation time loss could be up to one BUSCLK -cycle. The READY- delay logic on a slave module must be designed such that the number of selectable BUSCLK- delay cycles is one more than the maximum access time. For example, if the maximum access time is 400 ns and the BUSCLK- frequency 10 MHz the minimum number of selectable cycles must be five.

3.4 SYSTEM INITIALISATION

In a Multi-Microcomputer system initialisation can occur via the non maskable interrupts NMI- or RESET. Initialisation using RESET is recommended when fixed vectors in EPROM are available (address hex 0000 to 007E). In solely RAM based systems a cold start via the NMI- vectors by means of a loader (e.g. loading of the operating system from floppy or cassette memory) is advisable. In a system with several MMC-modules it is necessary to determine whether parallel initialisation of all MMC-modules via PRES- or NMI- should occur, according to the relevant tasks. Loosely coupled intelligent control units are initialised using their own switch on delay (power on reset) and/or IORST-. Software initialisation should be provided to initialise individual units or groups of units.

In E-Systems providing data integrity in non-volatile memories or battery back up RAM the mains failure interrupt, PWRFAIL-, should be evaluated by the CPU. To enable an interrupted program to be restarted automatically once mains is restored, important data should be first stored just prior to supply failure. The state of the PWRFAIL- line must therefore be monitored by MC or MMC-modules.

When only a momentary mains interruption occurs, a direct restart of the interrupted program can be performed. The time period during which PWRFAIL- is active before the supply voltages fall below their nominal tolerance depends very much on the form of PWRFAIL- recognition, supply reservoir capacitance and the loading. In E-Systems the minimum period is specified as 20ms. In the case of a program which cannot be safely interrupted for the duration of a "short mains failure" a total hold or wait state must be introduced after the maximum allowable "disconnection" time. If all the necessary information is stored for a correct restart then a mains failure flag can be set and the program can jump to a wait loop (e.g. PWRFAIL- request or IDLE command).

If the system supply voltages go outside their prescribed tolerance then PRES- becomes active and prevents invalid cycles during switch off. If the supply voltage returns, the program is started via the reset vectors following the switch on delay.

If the system is powered up for the first time or is reinitialised this is known as a "cold start". This can be performed using the NMI- vector to differentiate it from a warm start following mains failure. Fig. 3-14 shows the relationship of cold and warm starts in the form of a flow diagram.

In MMC-systems the IORST-line must be driven by only one MMC-module and thus must be jumper selectable.

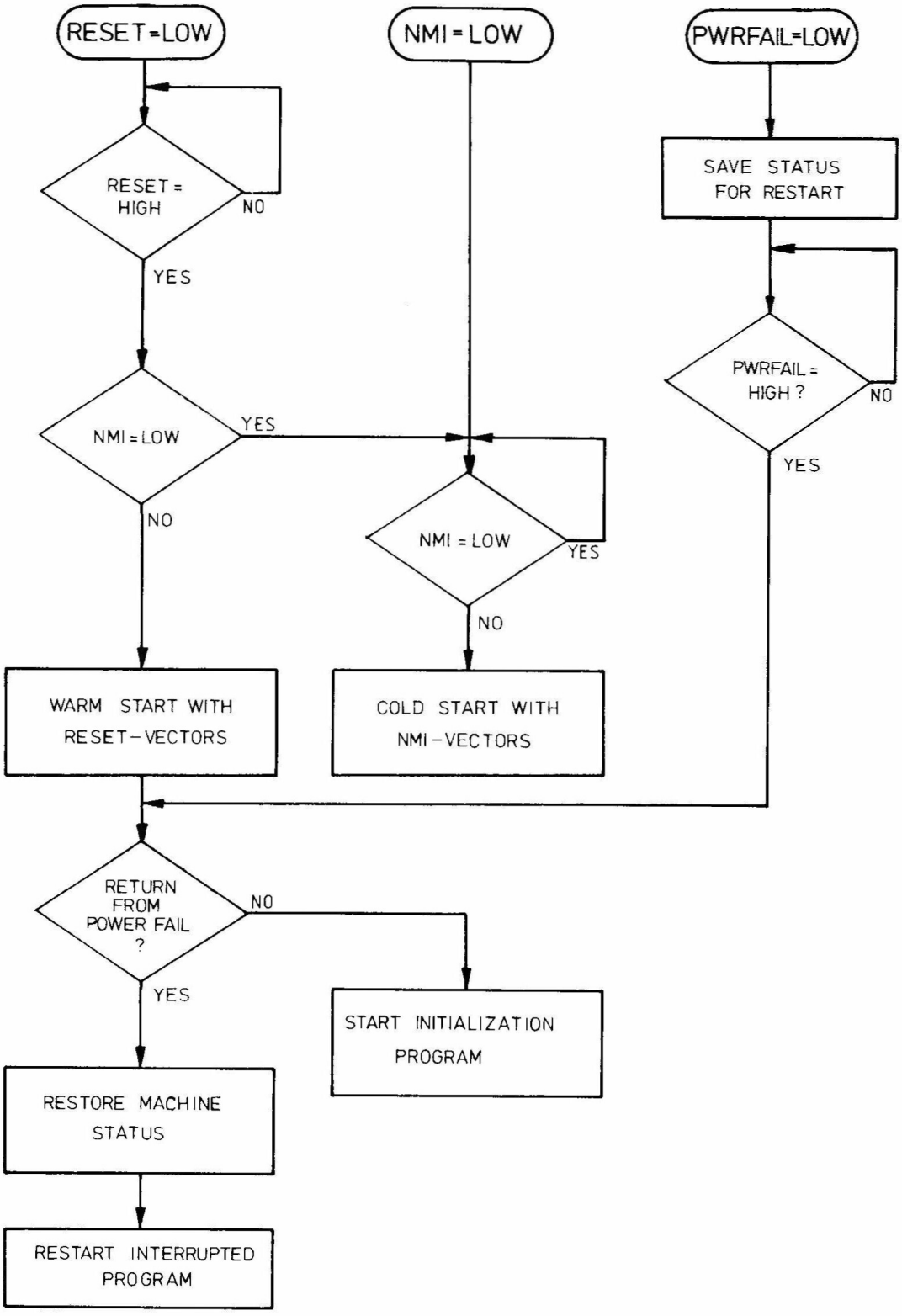


Figure 3-14 Cold and Warm Start via NMI- and PRES- Interrupts

3.5 INPUT/OUTPUT STRUCTURES IN MULTIMICROCOMPUTER SYSTEMS

In order to maximise the cost effectiveness of input/output modules, E-BUS supports the following I/O interfaces:

- bit serial programmable input/output (CRU)
- parallel byte or word input/output
- direct memory access (DMA)

In multi-microcomputer systems the address space of the input/output interface available to each microprocessor must be divided into:

- private input/output ranges
- common input/output ranges

Private input/output ranges can be further subdivided into units which are connected to E-BUS (tightly coupled) and units which are connected to a local bus. The advantage of local input/output is that no E-BUS loading occurs during data transfers. The range of private input/outputs is however often severely limited by module dimensions. If private input/output modules are connected to E-BUS then loading of the bus occurs through tightly coupled input/output operations. Therefore private input/output modules should only be used on E-BUS when the :

- bus loading is sufficiently low
- tight coupling is required to ensure correct operation in an error condition (e.g. via another MMC-module)

3.5.1 LOCAL INPUT/OUTPUT EXPANSION

If the private input/output on an MMC-module is to be expanded then a local or "private E-BUS" may be used to communicate to further input/output modules. Since E-BUS only requires a single 64 pin connector a private E-BUS can be realised on a double Eurocard board by using the second connector. Fig.3-15 shows a possible arrangement when using the double Eurocard format. Communication to local input/output devices or lines occurs via the two front connectors (max. 2 x 96 connections). The back plane for connector A may be used for E-BUS giving complete multiprocessor capability while connector B is used for a private E-BUS.

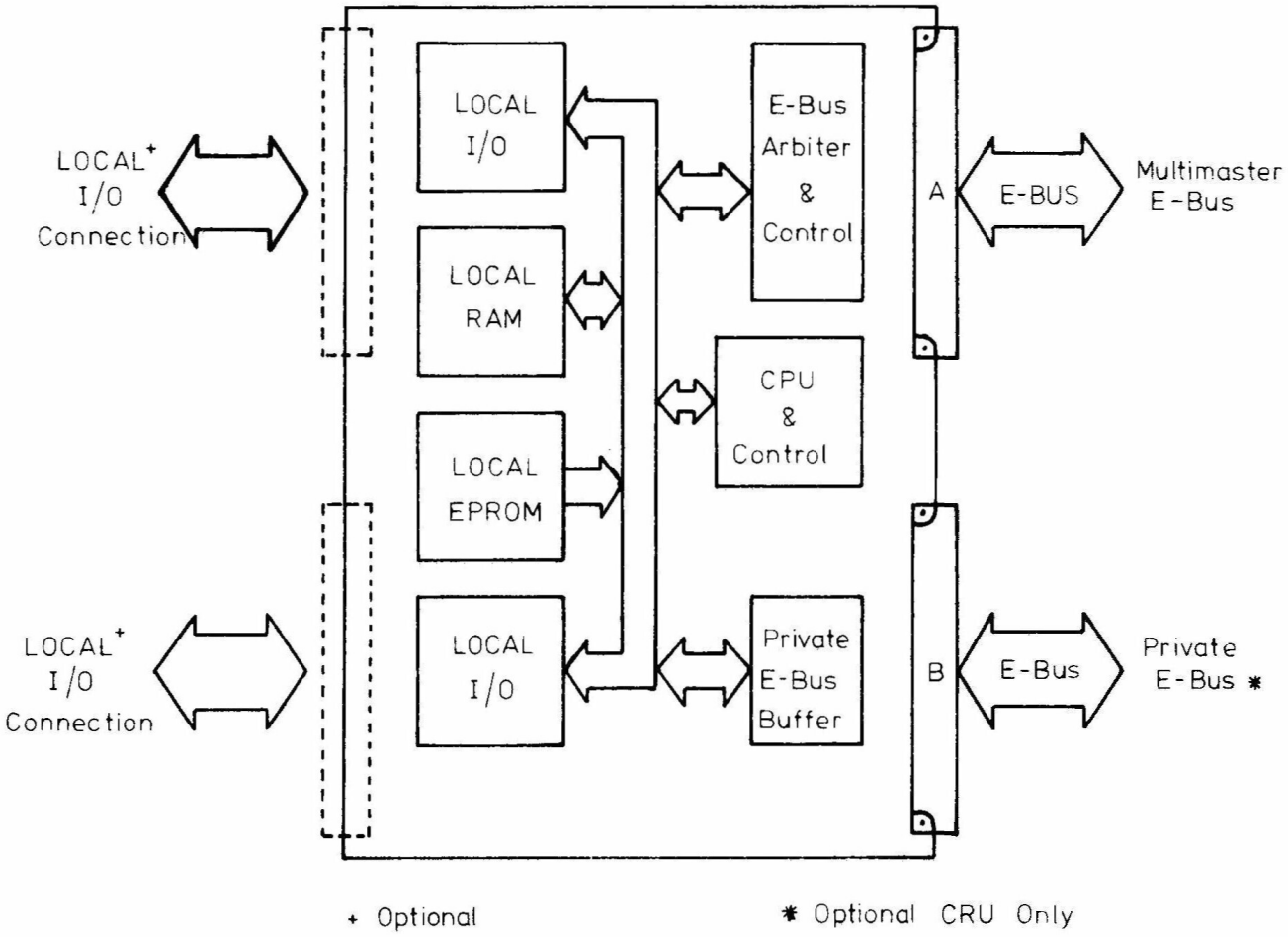


Figure 3-15 Local Input/Output Expansion for MMC Modules

In the simplest case the "private bus" can consist merely of the CRU interface of the 99XXX microprocessors; then only the following lines are required:

Line	No.	Comment
- A0-A14,A15/CRUOUT	16	Address line
- CRUIN,CRUCLK-	2	Data/clock line
- IORST-,BUSCLK-	2	Clock/reset line
- BUSY-,GRANTIN,GRANTOUT INTEN-	4	Interrupt control *

* only required for complete interrupt control

If no interrupts are required then the lines GRANTIN, GRANTOUT and INTEN- can remain disconnected. However BUSY- must then be set LOW to prevent bus arbitrations by the interrupt logic on standard modules. If parallel input/output modules or local memory expansion is desired then a complete E-BUS interface should be provided. In this case all the standard E-BUS modules, for example memory and input/output expansion modules, may be used without limitation on the "private E-BUS".

The back plane assembly described in section 2.5.4 relating to MC systems is sufficient for the private E-BUS.

3.5.2 E-BUS OVER SEVERAL CHASSIS

If, in an industrial application, the use of a large number of central input/output modules is required in the system, the use of several 19" chassis is often inevitable. Unfortunately the implementation of a multiprocessor E-BUS over several chassis incurs a greater expense. In this case a functional division of the application into main and subsystems with individual intelligence is recommended. The coupling can be loose or tight as required. The simplest extension to E-BUS is provided by a tight coupling of the bit serial input/output (CRU) over two or more chassis. Buffering must be provided between the chassis. An expansion of only one chassis (line length <1m) is possible with the TM990/E150/1 MC-modules because of the maximum permissible signal cycle time in conjunction with the TMS9901/ 9902/9903/9911 LSI input/output devices. If purely TTL input/output devices (e.g. SN74LS245 or ´LS259) are used to realise the bit serial CRU interface then an expansion by two chassis is possible (line length <2m). If a distance of up to 30 meters needs to be covered between two chassis then this can be achieved using the new 99XXX microprocessors (e.g. TMS9995 or TMS99105) since the new processors allow the speed of the CRU interface to be altered by use of the READY- line such that longer signal cycle times are permissible. Fig.3-16 shows a block diagram of this form of CRU interface between E-BUSes. The signal lines must be terminated at each end with the characteristic impedance of the line to avoid reflections.

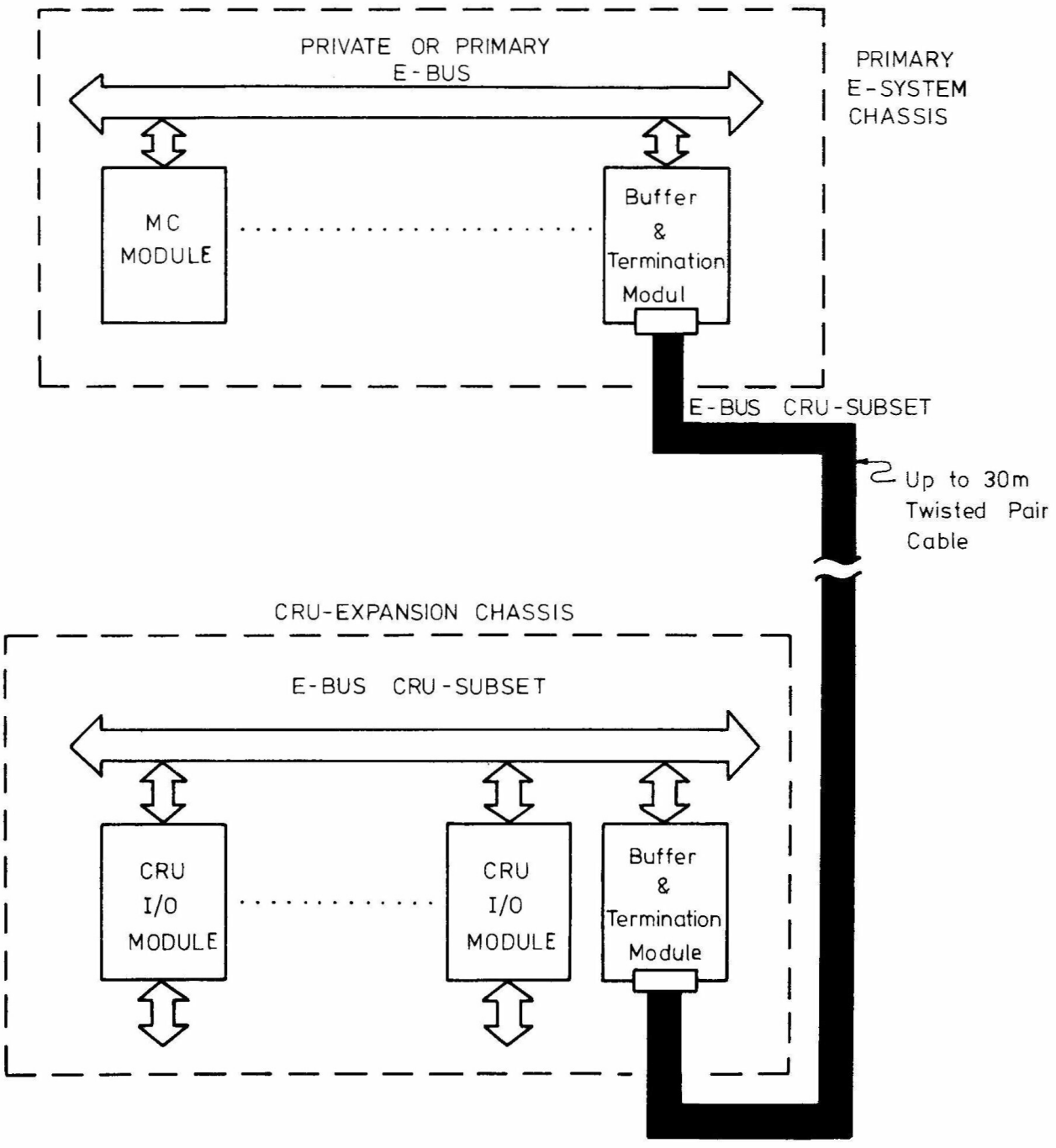


Figure 3-16 Coupling of Separated Chassis via the E-BUS CRU Interface

If two separated chassis are required to be interlinked in an electrically noisy environment then differential line drivers and receivers should be used (e.g. SN75107-112 or RS422 driver). It is also possible to completely isolate the CRU

interface using opto couplers provided the bit transfer rate is compatible with the speed of the opto coupler (correspondingly more wait states provided using READY-).

It is recommended that tight coupling of E-BUS chassis is only used for single microcomputer systems having low speed requirements or MMC-modules with "private E-BUS" facilities (see section 3.5.1). Limiting the data rate of the CRU interface has the effect of producing a higher loading on E-BUS. The optimum solution is to couple distant E-BUS chassis (<30m) using an intelligent input/output module which is in turn loosely coupled to the primary E-BUS.

The extension of E-BUS for the control of parallel input/output modules may be performed in the same manner as for the bit serial CRU interface, however the expense for lines and transceivers is increased.

If distances greater than 30m are to be covered then loose coupling using a standard serial interface is recommended (see section 3.1.2).

For expansion chassis which also house A/D and D/A modules, communicating via the bit serial CRU interface, the E-BUS signals ANALO, ANAHI and ANACO can be used to interface to analogue multiplexer modules (see section 2.3.5).

3.5.3 CONTROL OF COMMON INPUT/OUTPUT UNITS

If common input/output units are tightly coupled within an E-BUS multi-microcomputer system then the system hardware and software must ensure that no bus blocking occurs. This section describes in general terms what is required to achieve this. To prevent the common input/output units (e.g. floppy disc control unit) being simultaneously accessed by two or more MMC-modules, control flags must be generated in common system memory. As in the synchronisation of parallel software processes, the control of common input/output units uses a system of "semaphores". A semaphore is a memory word in the common system memory which specifies the state of an I/O module. If the semaphore is inactive (e.g. hex FFFF) then the associated I/O module is available (not occupied at that time). An active state (e.g. hex 0001) signifies it is occupied. If the software in an MMC-module wishes to access a common I/O module it tests the relevant semaphore for an inactive state. If it is found to be inactive then the software sets the semaphore active. If the semaphore is found to be already active however, the software must wait until the I/O module is free.

In the 99XXX microprocessors the ABS (set absolute value), TSMB or TCMB command is used to test the semaphore (test and set if inactive). Since each microprocessor command consists

of a sequence of internal operations and external memory cycles it must be ensured that between the period of testing the semaphore and setting it (if possible), no other MMC-module accesses the semaphore. This is assured by the MMC-module microprocessor producing a signal to the bus control to lock the E-BUS to all other modules (bus lock) during the semaphore test. If this signal is not produced by the microprocessor itself it can be produced by external decoding or by setting/resetting using input/output commands.

Fig.3-17 shows a software flow diagram for the semaphore test in a real time system.

Release of the common I/O module is achieved using a simple set command (e.g. SETO SEM1 on TMS99XXX).

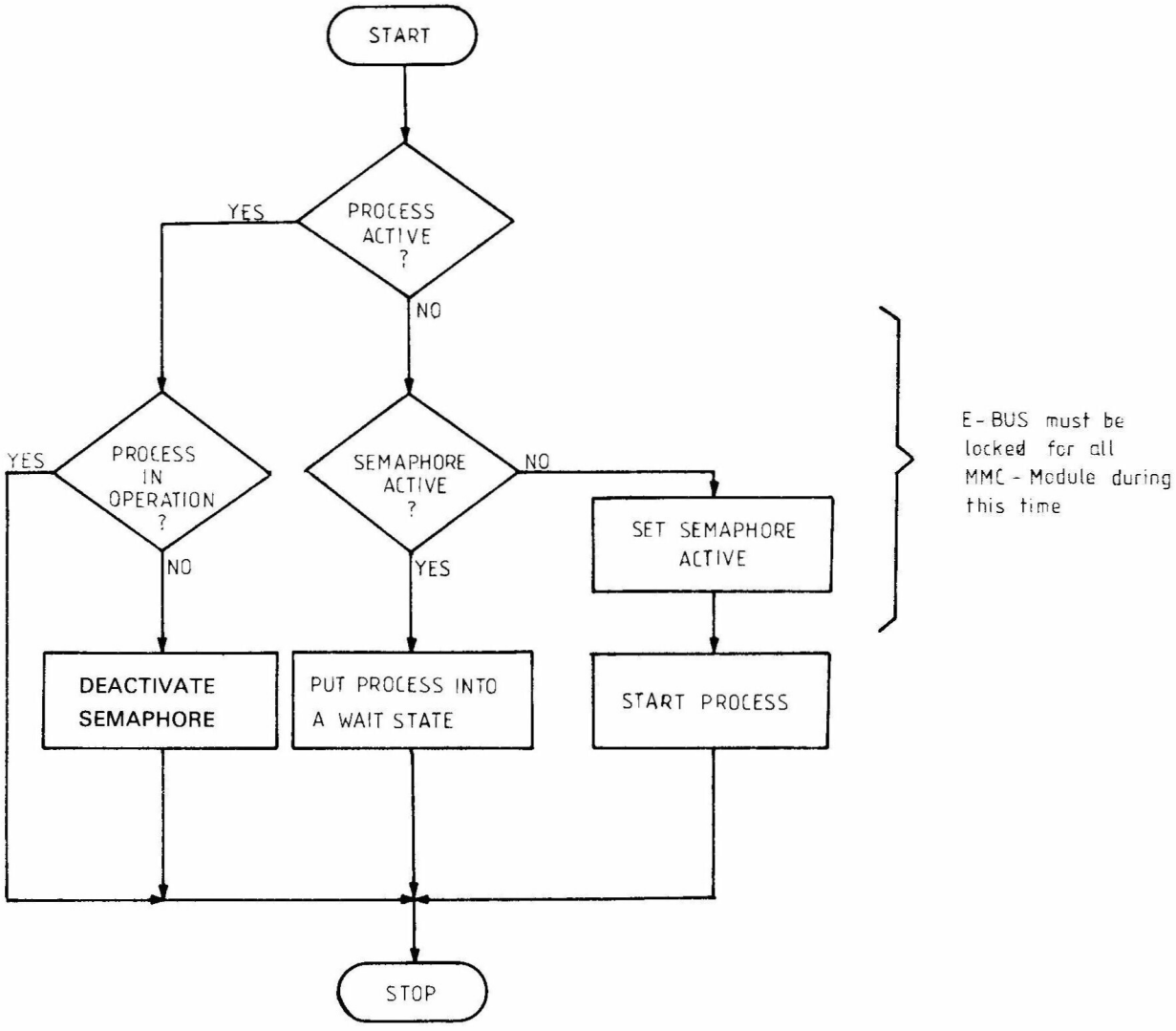


Figure 3-17 Semaphore Control for Common I/O Modules

SECTION 4

MEMORY EXPANSION

The following section of this handbook illustrates, by use of examples, the development of memory and memory mapped I/O modules which are electrically and logically compatible with E-BUS.

Suggestions for module development and specific E-BUS timing information are given.

4.1 SIGNAL DESCRIPTION

The control signals used by E-BUS to control a module are described below. In this section only the E-BUS signals relevant to memory expansion modules are described (see also section 2.3.3.1).

4.1.1 ADDRESS AND DATA BUS

A0/D0-A15/D15: Multiplexed address and data bus, where A0/D0 is the MSB and A15/D15 is the LSB.

XA0-XA3: Extended address lines XA0 (MSB) to XA3 (LSB), non-multiplexed.

4.1.2 CONTROL SIGNALS

ALATCH: The ALATCH signal indicates which information is transmitted on the multiplexed address and data bus (HIGH = address, LOW = data).

MEMEN-: MEMEN- is always active (low level) when a memory cycle is in progress.

WE-: WE- signifies a write cycle. During the active phase (low level) data is transmitted from the master to the memory module. This bus signal can be connected to the WE- inputs of memory components after suitable buffering.

DEN-: During the active phase of DEN-, data is transmitted from the memory to the master module, i.e. a read cycle is

performed.

READY-: Data ready signal. Data is valid during the present BUSCLK- cycle. The memory cycle will be concluded after the present BUSCLK- cycle.

AREADY-: Data ready signal. Data will be valid during the course of the next BUSCLK- cycle. The master module can only complete the memory cycle after the following BUSCLK- cycle.

BUSCLK-: System clock. When using the TM990/E150 MC-module the system frequency is 2.5MHz, and with the TM990/E155 it is 3MHz.

MEMWIDTH: On E-BUS 16 bit data words can be transmitted on an 8 bit wide data bus (AD8-AD15) in two memory cycles or on a 16 bit wide data bus in one memory cycle. The data bus width is indicated by the MEMWIDTH signal (HIGH = 8 bit width, LOW = 16 bit width).

4.1.3 CONTROL SIGNALS FOR BATTERY BACKUP SYSTEMS

PRES-: The PRES- signal is actived (set to low level) as soon as one of the supply voltages falls out of its nominal tolerance range. Following the power up of the system, the PRES- signal remains active until all voltages have achieved their nominal values.

PWRFAIL-: The PWRFAIL- signal is actived (set to low level) 20ms before one of the supply voltages falls out of its nominal tolerance range.

+5VSTBY: This line is supplied with a regulated +5V voltage which remains at a constant +5V level even on mains failure.

+BATT: The bus line +BATT is provided to supply the system with an unregulated battery voltage.

The E-BUS lines PRES-, PWRFAIL- and +BATT are specified by Texas Instruments but are not supplied by the MC-module or other modules; instead they must be produced by the power supply. Section 4.7 gives the timing information for these signals.

4.2 ADDRESS AND DATA BUS INTERFACE

4.2.1 BUS INTERFACE REQUIREMENTS

One requirement of the bus interface is to minimise the loading of the bus lines. As a guide a loading of 2 ´LS inputs should not be exceeded at one interface to E-BUS. If this is not possible then the total loading on the bus must be calculated for a given system to ensure that the drive capabilities of possible bus master modules are not exceeded (see section 2.5.6).

As well as minimising the bus loading the bus interface undertakes the demultiplexing of addresses and data, as well as switching the data driver from read to write operation as required.

4.2.2 REALISATION OF THE DEMULTIPLEXER

As the signal ALATCH indicates whether data or addresses are being transmitted on the bus this signal can also be used to store the address. The address bits are stored in latches until the occurrence of a new memory cycle. If ALATCH is active (high level) the latches are accessed, i.e. transparent, in order to route the address to the decoder logic with the minimum possible delay. The address is latched in on the falling edge of the ALATCH signal.

Minimal delay to the address is necessary since the time between presentation of the address and the return of the READY- (or AREADY-, as required by the TM990/E150 module) is extremely tight. A component eminently suitable, as it has a very short propagation delay time and presents minimal loading to the bus, is the SN74S373 (see table 4-1). The ´S373 is a transparent 8 bit latch having control inputs OC (OUTPUT CONTROL) and G (ENABLE). G can be directly connected to ALATCH since the ´S373 is transparent when a high level is present at G and data is latched on a negative going edge at this input. The control inputs of the ´S373 are buffered via Schmitt-Trigger input gates for increased noise immunity, hence increasing rejection of any noise present on the bus. A Schmitt-Trigger input buffer is required if ALATCH is required to drive more than two UBL loads.

SN74S373	
HIGH LEVEL INPUT CURRENT	50uA
LOW LEVEL INPUT CURRENT	-250uA
MAXIMUM DELAY TIME	18ns
SN74LS245	
HIGH LEVEL INPUT CURRENT	20uA
LOW LEVEL INPUT CURRENT	-200uA
HIGH LEVEL OUTPUT CURRENT	-15mA
LOW LEVEL OUTPUT CURRENT	24mA
MAXIMUM DELAY TIME	40ns

Table 4-1 ´S373 and ´LS245 Technical Data

4.2.3 CONTROL OF THE DATA DRIVER

The same selection criteria exist for the data driver as for the address latch, namely, minimum propagation delay time together with minimum bus loading. The data driver should also be bidirectional and have 3-State outputs. A suitable device is the ´LS245 (see table 4-1), which is an octal bidirectional driver having control inputs G and DIR. DIR controls the direction of the driver and is connected to the bus signal DEN-.

The simplest solution for the control of the ENABLE input would be the gating of ´BOARD SELECT´ with ALATCH to produce a ´BOARD ENABLE´ signal to control the driver. This however would result in a data bus conflict during the write cycle since the memory is only in write mode during the active phase of WE-, and the internal driver of the memory is switched into read direction, towards the data driver (see fig.4-1), before and after the WE- pulse.

After buffering, the WE- bus signal can be used directly to control the memory components.

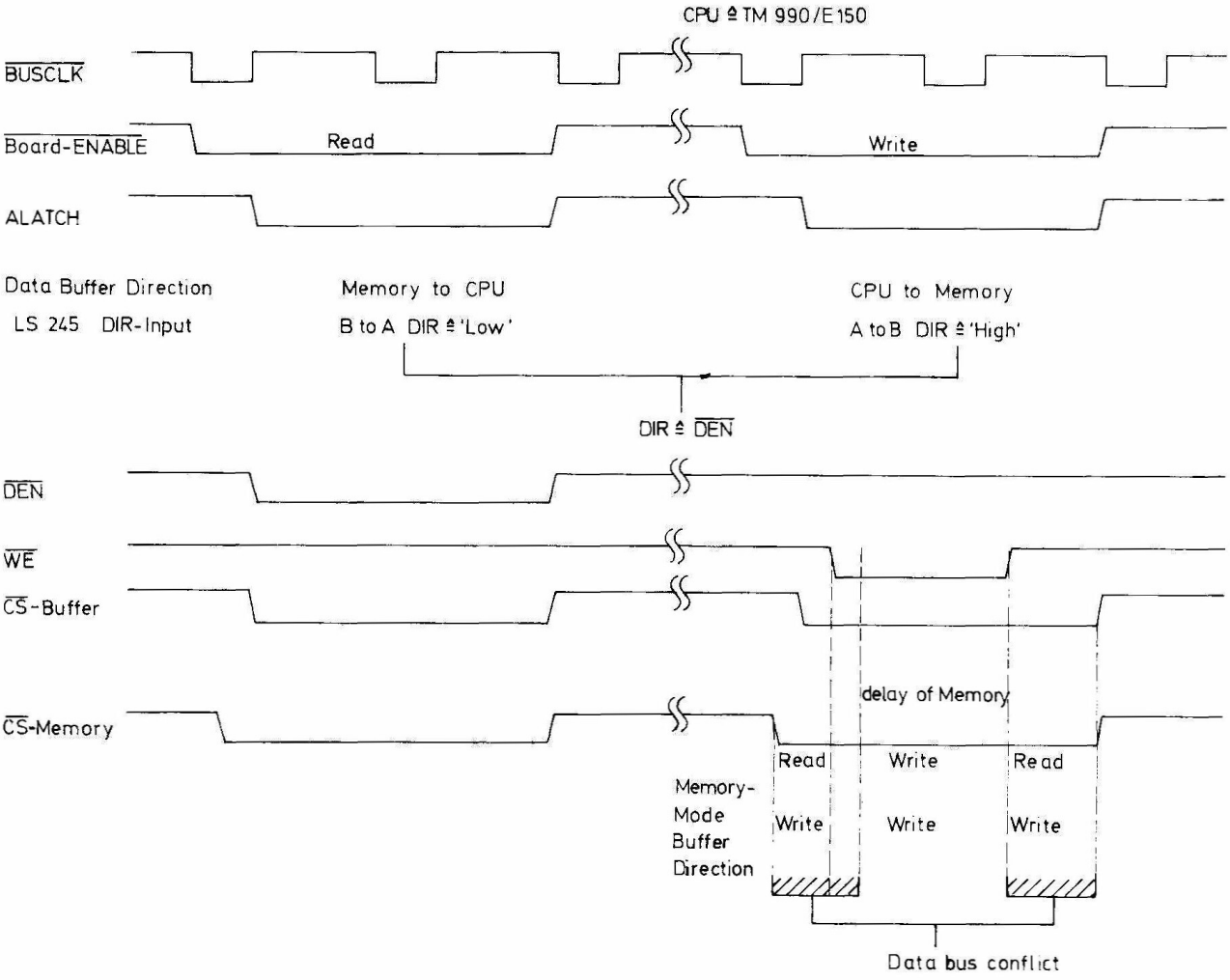


Figure 4-1 Data Bus Conflict

A partial solution to the data bus conflict is to gate the signals DEN- and WE- with the generated 'BOARD ENABLE' signal. Use of the resultant as the data driver enable signal reduces the data bus conflict.

If the enable input to the memory components is similarly controlled then the data bus conflict is resolved completely (see fig.4-2 and 4-3). The timing requirements of the memory components' enable inputs are not critical since the memory access time from presentation of the address is significantly longer than that from presentation of the enable signal.

e.g.: TMS2114-45, taad 450ns and tacs 120ns

taad = access time from addresses

tacs = access time from CS

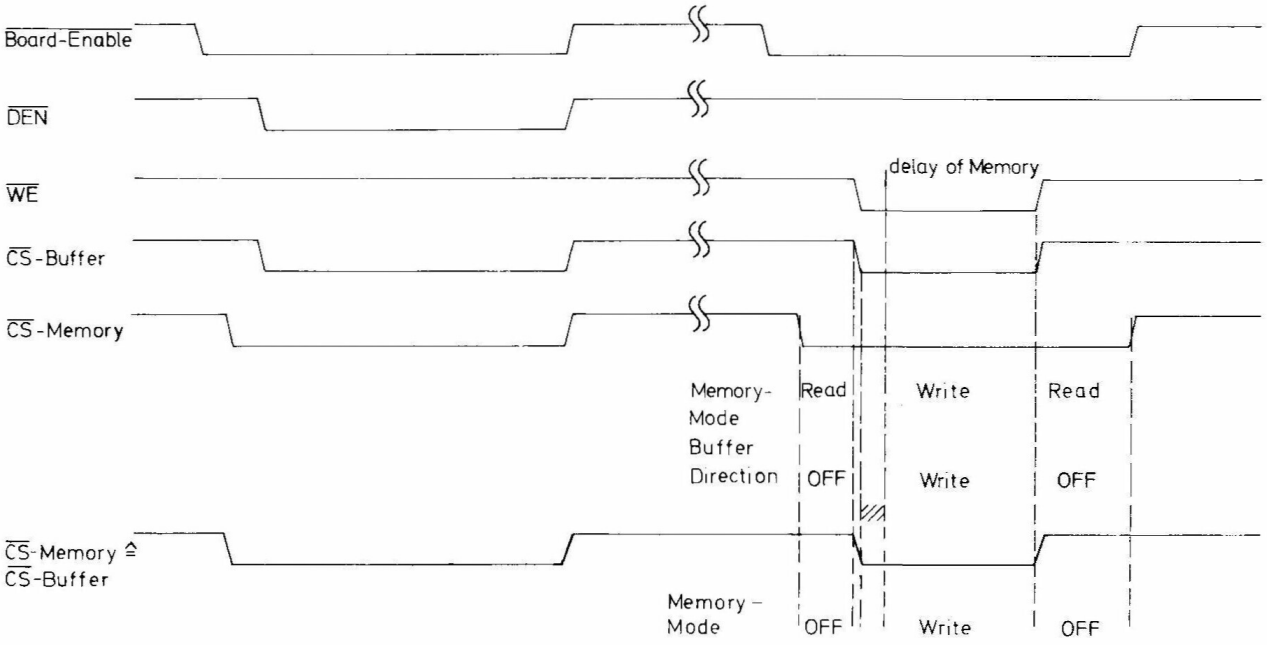


Figure 4-2 Memory Control without Data Bus Conflict

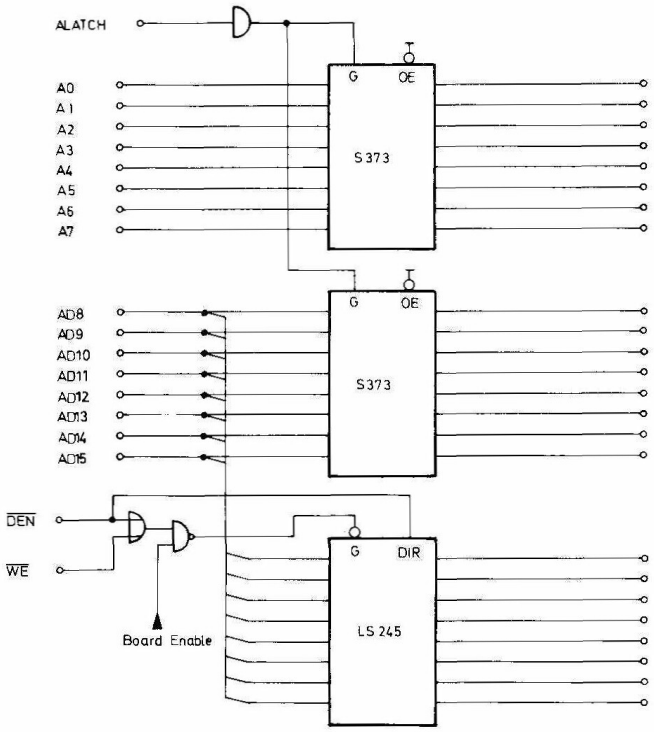


Figure 4-3 Data Driver Control

4.3 ADDRESS DECODING

To achieve optimum use of the available address space, the complete address (20 bits) must be decoded for each module. The remaining address space is then available for other applications and double addressing is avoided. The address decode logic produces the BOARD ENABLE signal which is then used to produce the READY- signal and the ENABLE signals for memory.

4.3.1 ADDRESS DECODING REQUIREMENTS

The total address space must be decoded to produce the necessary address range, i.e. not only the 16 address bits A0 - A15 but also the extended address bits XA0 - XA3. These address bits are required for operation of future CPU modules. For standard modules with less than 16k byte capacity the start address of the address space of the memory module must be relocatable in 2k byte steps within the total address space. If realisation of this requirement is not

feasible then the address block should be relocatable to the largest degree possible within the total address space. This requires that the start address can be relocated in steps which are as small as possible, resulting in the greatest flexibility and allowing optimum use of the available address space.

4.3.2 DIFFERENT TYPES OF ADDRESS DECODING

Of the various different types of address decoding four methods are described below and are explained using circuit examples.

- address decoding using fixed combinational logic
- address decoding via information stored in a PROM
- address decoding using a comparator and DIL switches
- address decoding using an adder and DIL switches

4.3.3 FIXED COMBINATIONAL LOGIC OR PROM

When using combinational logic for address decoding the address bits used are suitably gated such that the output only becomes active on a certain address word. The output then becomes the BOARD ENABLE signal. This solution to address decoding is simple to construct and has a relatively short delay time. The disadvantage lies in the fact that the module address can only be altered by modifications to the module itself. Thus a large part of the requirements mentioned above is not fulfilled in that the system offers little or no flexibility in memory relocation.

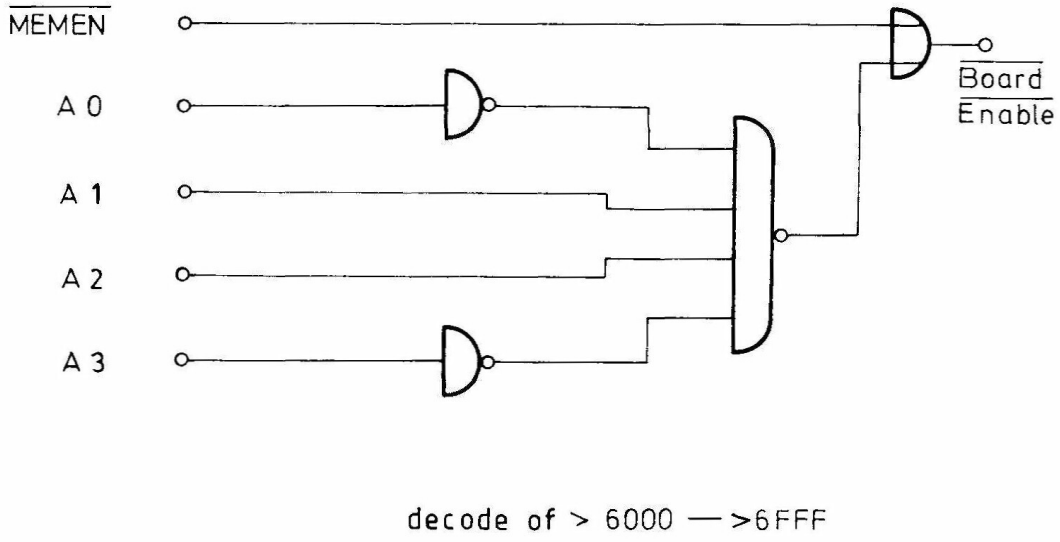


Figure 4-4 Address Decoding using Combinational Logic

If a PROM is used to facilitate decoding then the start address may be altered by reprogramming the PROM. Alteration of the start address of the memory expansion module through reprogramming of the PROM is not however particularly flexible during development phases.

4.3.4 COMPARATOR WITH DIL SWITCHES

The comparator compares the value entered by means of the DIL switches with the address and produces a BOARD ENABLE signal when these concur. This system fulfills most of the ideal requirements of the address decoder since the start address is easily relocated with the aid of the DIL switch. The disadvantage of this solution is that the smallest decoded block of addresses is always as large as the address space required by the module. The start address can therefore only be changed in blocks corresponding to the total address space required by the memory module.

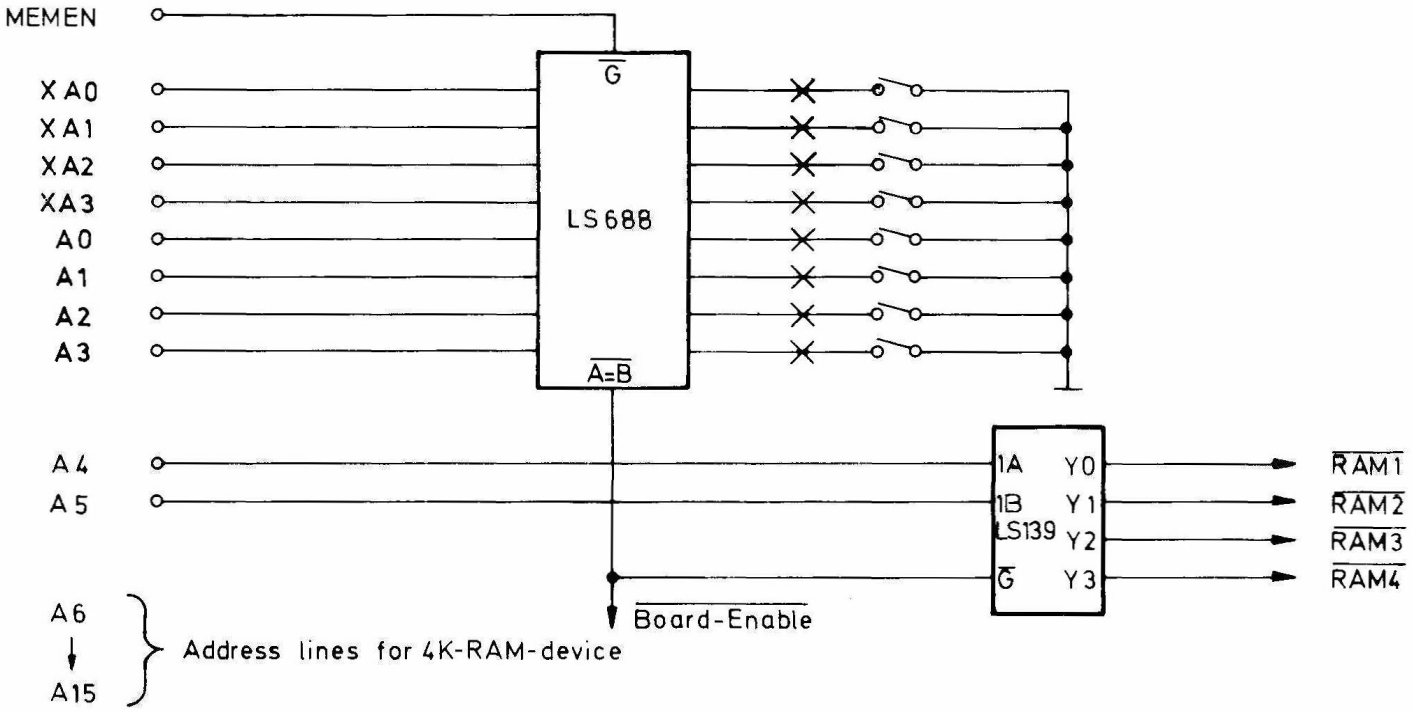


Figure 4-5 Comparator with DIL switches

Suitable components for the realisation of this type of address decoding are the SN74LS85 4 bit comparator or the SN74LS688/682 8 bit comparator. The SN74LS682 has internal pull up resistors eliminating the requirement for external components. In order to achieve a minimum delay time it may be necessary to use Schottky components in place of Low Power Schottky devices. The application of Schottky devices is particularly necessary for the decoding of the BOARD ENABLE signal used to produce the READY- signal. Another alternative for use in future developments is provided by the ALS series, which offers the speed of Schottky with a much lower power consumption.

4.3.5 ADDER WITH DIL SWITCHES

The adder forms the sum of the value presented by the DIL switch and the address word. If all the sum outputs are at a logic one then a BOARD ENABLE signal is produced.

If address bits represent small increments within the necessary address range, then the start address can be moved in blocks which are smaller than the total address space required by the memory module. In this case the lower order bits of the sum output are used for generating addresses within the memory module address space.

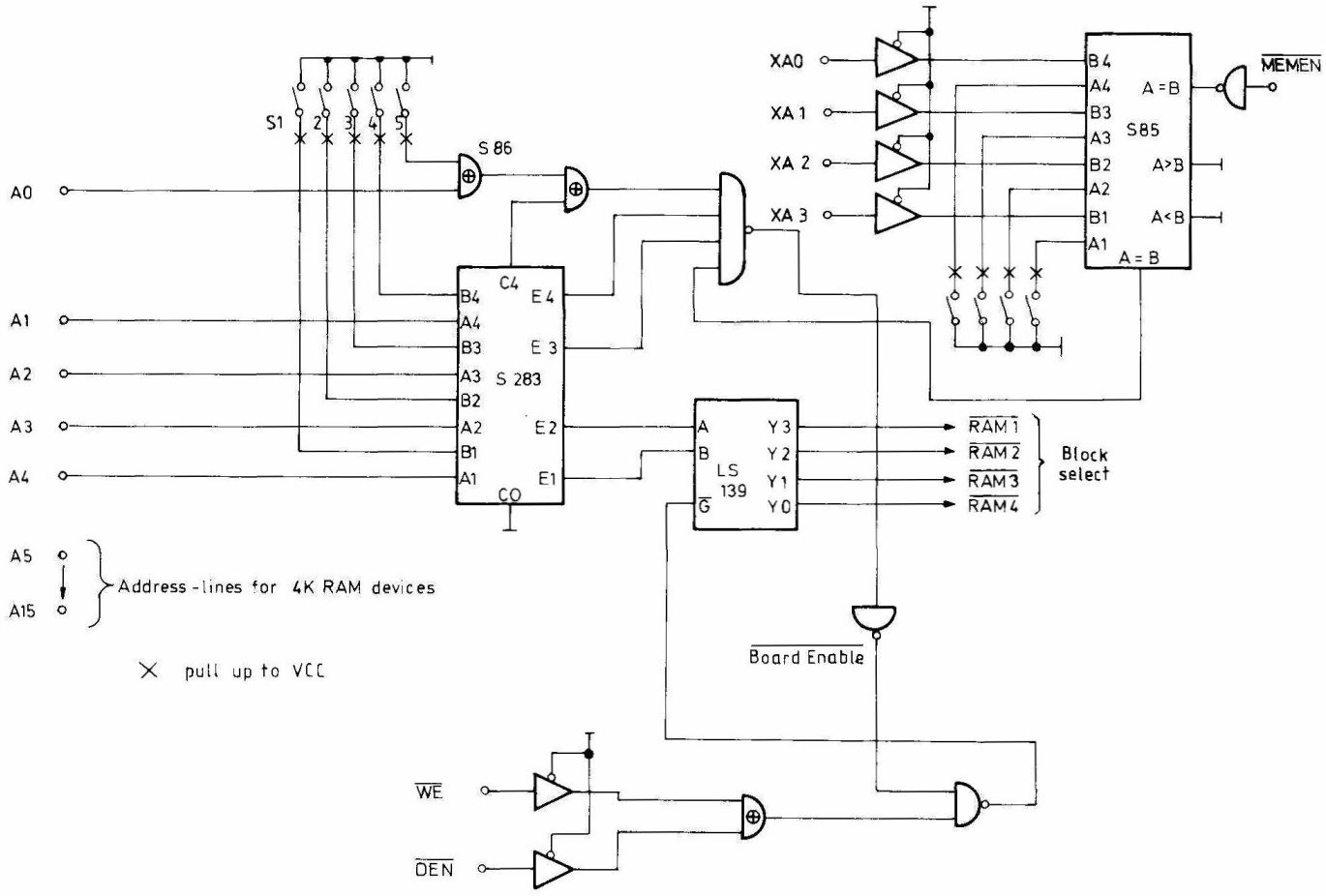


Figure 4-6 Adder with DIL switches

The decoder logic shown in fig. 4-6 covers a total range of 1 Megabyte. The memory block is 8k bytes long and is addressed by address bits A3 - A15. This address space is divided into 2k byte blocks which are addressed by address bits A5 - A15. In order to achieve this address bits A0 - A14 are connected to the 'S283 adder and the start address is controlled by the quintuple DIL switch. The three highest order bits are gated to produce the BOARD ENABLE signal while the two lowest order sum outputs address one of the four 2k byte memory blocks according to the switch positions along with the presented address.

Example 1:

	A0	A1	A2	A3	A4
ADDRESS	0	0	1	1	1
DIL SWITCH	1	0	1	0	1
SUM	1	1	1	0	0

BOARD - SELECT BLOCK 1

Example 2:

	A0	A1	A2	A3	A4
ADDRESS	0	1	0	1	0
DIL SWITCH	1	0	1	0	1
SUM	1	1	1	1	1

BOARD - SELECT BLOCK 1

When using this solution care must be taken to minimise the propagation delay time. It is recommended that a Schottky device (SN74S283) is used as an adder or that a half adder be discretely constructed using the SN74S86 EXCLUSIVE OR gate.

TM990/E251 MEMORY MAP

FROM	TO	S1	S2	S3	S4	S5	
>0000	>1FFE	0	0	1	1	1	NOTE : "OPEN" = 1
>0800	>27FE	1	1	0	1	1	
>1000	>2FFE	0	1	0	1	1	
>1800	>37FE	1	0	0	1	1	
>2000	>3FFE	0	0	0	1	1	
>2800	>47FE	1	1	1	0	1	
>3000	>4FFE	0	1	1	0	1	
>3800	>57FE	1	0	1	0	1	
>4000	>5FFE	0	0	1	0	1	
>4800	>67FE	1	1	0	0	1	
>5000	>6FFE	0	1	0	0	1	
>5800	>77FE	1	0	0	0	1	
>6000	>7FFE	0	0	0	0	1	
>6800	>87FE	1	1	1	1	0	
>7000	>8FFE	0	1	1	1	0	
>7800	>97FE	1	0	1	1	0	
>8000	>9FFE	0	0	1	1	0	
>8800	>A7FE	1	1	0	1	0	
>9000	>AFFE	0	1	0	1	0	
>9800	>B7FE	1	0	0	1	0	
>A000	>BFFE	0	0	0	1	0	
>A800	>C7FE	1	1	1	0	0	
>B000	>CFFE	0	1	1	0	0	
>B800	>D7FE	1	0	1	0	0	
>C000	>DFFE	0	0	1	0	0	
>C800	>E7FE	1	1	0	0	0	
>D000	>EFFE	0	1	0	0	0	
>D800	>F7FE	1	0	0	0	0	
>E000	>FFFE	0	0	0	0	0	
>E800	>07FE	1	1	1	1	1	WRAP-AROUND !!!
>F000	>0FFE	0	1	1	1	1	WRAP-AROUND !!!
>F800	>17FE	1	0	1	1	1	WRAP-AROUND !!!

Figure 4-7 Address Map for 8k Byte Memory

4.3.6 THE TM990/E250 MEMORY MODULE INTERFACE

A combined address decoding scheme is used on the TM990/E250 memory module (see fig. 4-8). Gates decode the extended address lines, while comparators handle address lines A0 - A3. Using comparators, two separate address ranges for EPROM and RAM addresses are decoded and an on board jumper allows the user to extend the EPROM address range from 4k bytes (TMS2532) to 8k bytes (TMS2564). In this case the start address can only be altered in 8k byte steps. The RAM address range has a size of 4k bytes while address lines A4 and A5 select a 1k byte block.

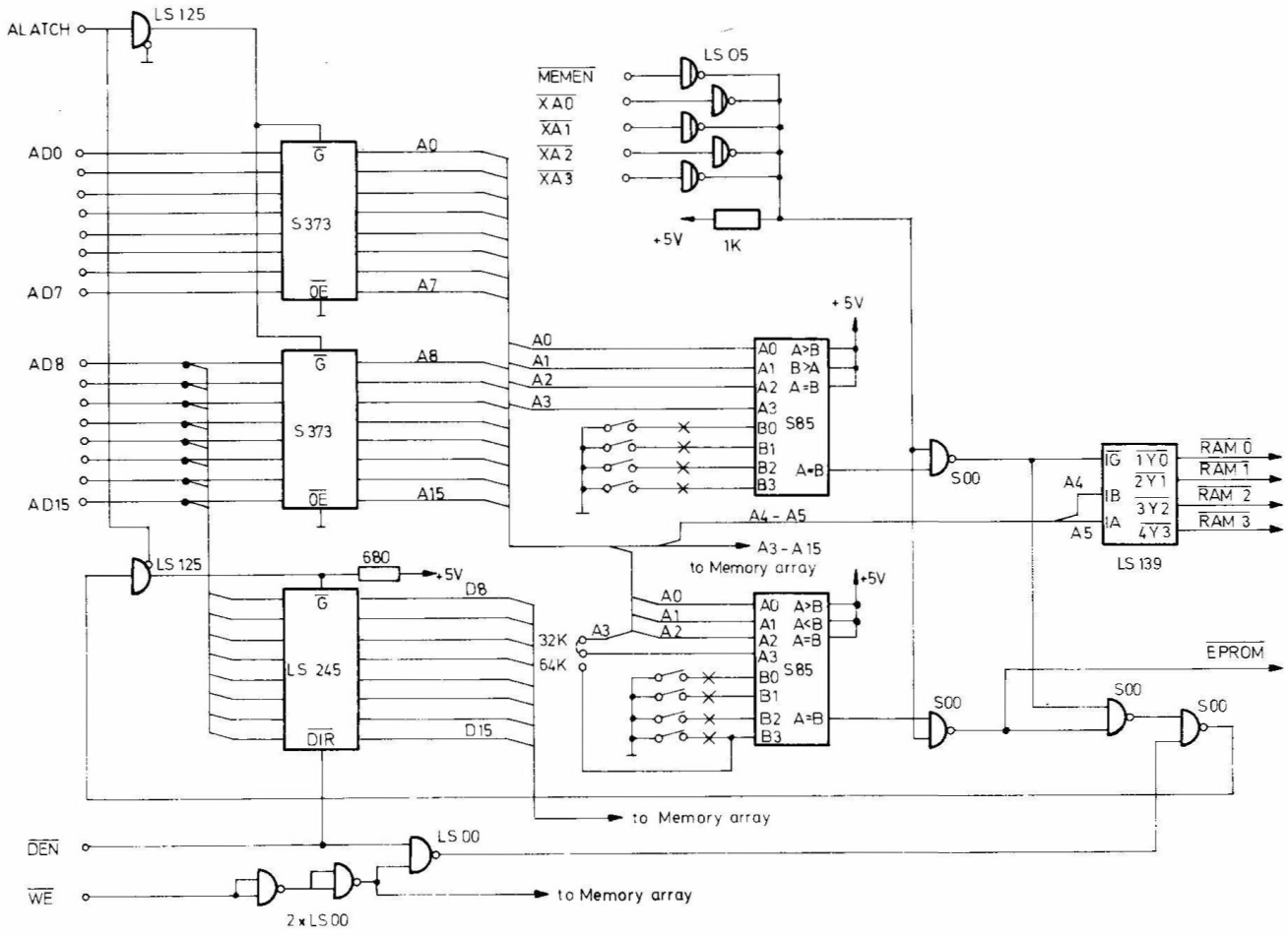


Figure 4-8 The TM990/E250 Memory Module Interface

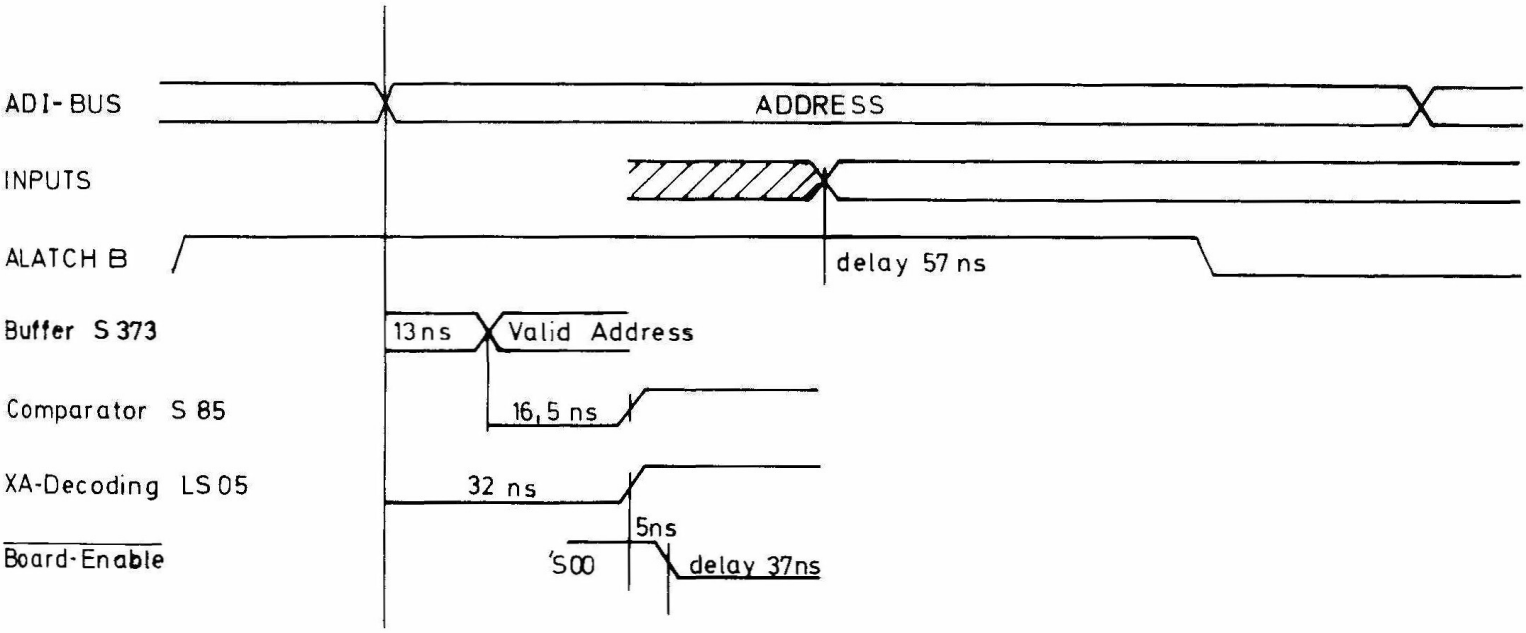


Figure 4-9 Timing Diagram for Bus Buffering and Address Decoding

The timing diagram shown in fig.4-9 shows the worst case timing from address presentation to a valid BOARD ENABLE signal.

4.4 READY- SIGNAL

E-Bus requires a READY- signal (active LOW) in order to complete a memory transfer cycle. If the addressed memory module does not send a READY- signal, the master module will insert wait cycles. If the processor addresses a non-existent memory location, there is a danger that the bus could hang up waiting for a READY- signal. To prevent this there is a bus timeout counter on the E5000 backplane that will activate READY-/AREADY- after a fixed number of BUSCLK-cycles (jumper selectable) if no memory module responds.

Two READY- lines exist on E-Bus; READY- and AREADY-. READY- is used if the data is present on the ADI-bus in the current BUSCLK- cycle. AREADY- indicates that the data will be present on the ADI bus in the next BUSCLK-cycle.

Memory modules must be able to drive both the AREADY- and the READY- signal. The MC-module TM990/E150 operates with the AREADY- and the MC-Module TM990/E155 with the READY- signal.

In order to achieve a fast memory cycle the timing requirements are tightly specified. The design of the bus interface and the decoding logic of a memory-module must be such that minimum time delays are achieved.

In single master systems the logical clock of the microprocessor is synchronous to BUSCLK-. Thus no synchronisation of the READY- signals is necessary if the set-up times of the microprocessor are met.

MEM-modules must meet the following worst case times if they are used together with the TM990/E150 or TM990/E155 MC-modules:

without wait states:	/E150	/E155
tar (valid address to valid READY/AREADY):	57ns	60ns
tad (valid address to valid data) Read:	400ns	97ns
tsuwe (data valid before positive WE- edge):	375ns	120ns

with wait states:	/E150	/E155
tcr (positive BUSCLK edge to valid READY/AREADY):	37ns	36ns
tcd (positive BUSCLK edge to valid data) Read:	440ns	72ns
tsuwe (data valid before positive WE- edge):	375ns	120ns

+ (no. of wait states) x (duration)

4.4.1 GENERATION OF THE READY- SIGNAL

READY- can be fed to the E-BUS asynchronously if no wait states are required. If the BOARD ENABLE signal directly drives the READY- line, via an open collector driver, it is mandatory that the relevant set up times for the MC-module used are met. If wait states are required READY- must be delayed by the positive edge of BUSCLK-, in which case the delay time from the positive BUSCLK- edge to a valid READY- must be such that the set up times of the MC-module are met (see section 4.4).

Fig. 4-10 shows the READY- logic of a typical MEM-module. A jumper gives the user the opportunity to choose between 0, 1 and 2 wait states.

The flip flops for the wait state generator are enabled by ALATCH = LOW and the READY- signal will be fed to the bus if a valid BOARD ENABLE signal is present. Alternatively the logical OR of WE- and DEN- can be used to enable the READY-logic.

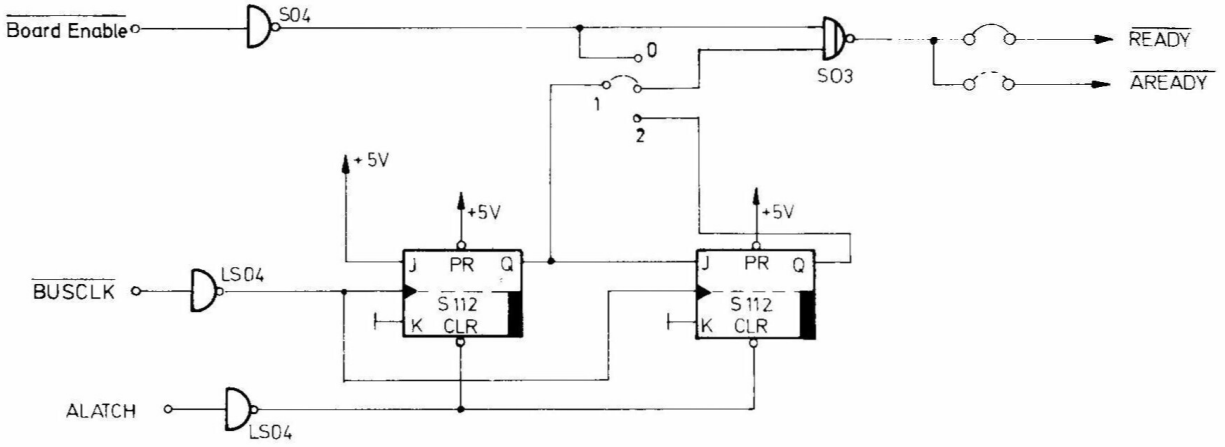


Figure 4-10 READY-Circuitry

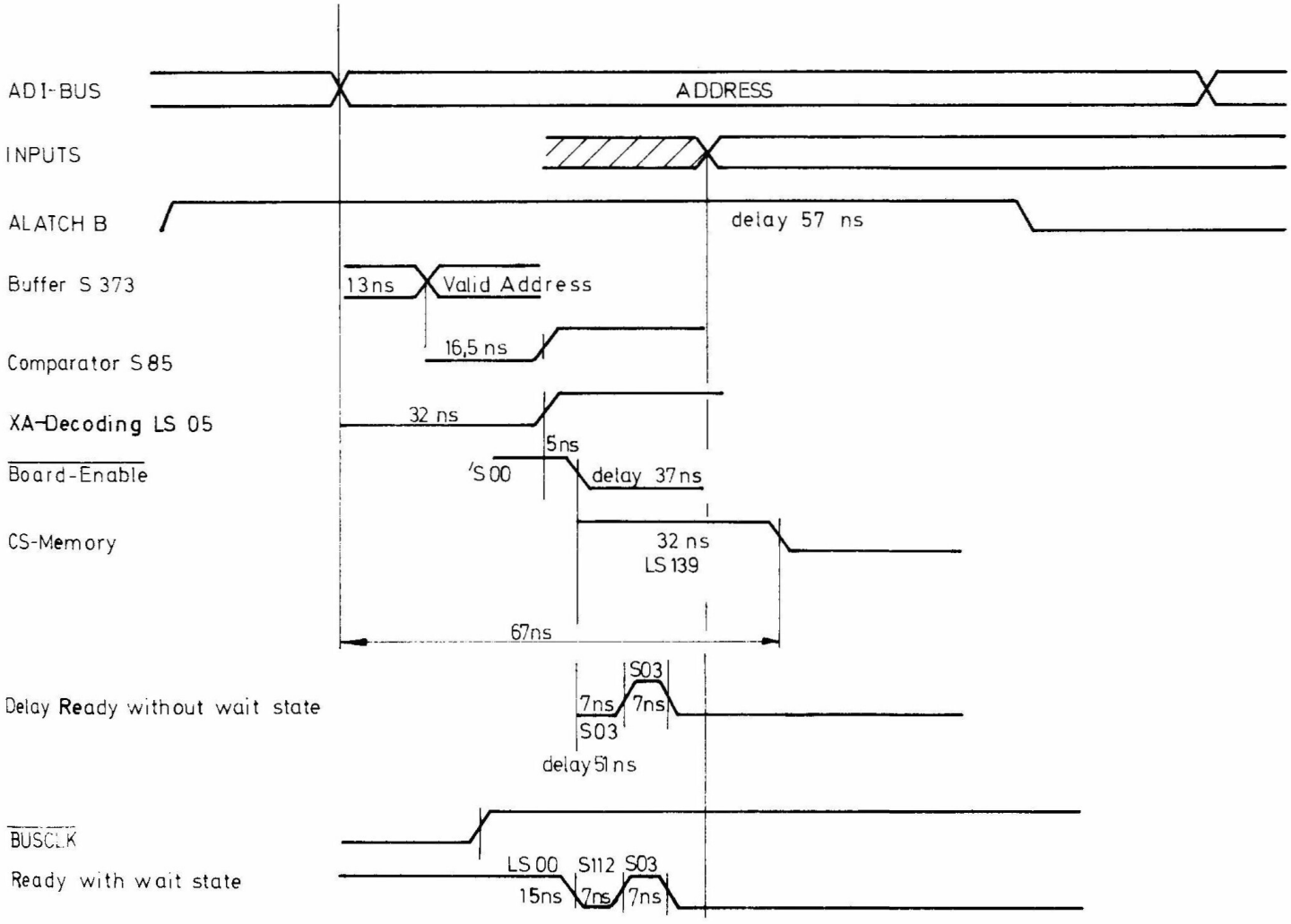


Figure 4-11 TM990/E250 Timing Requirements

The timing calculation for the MIO-module TM990/E250 in fig 4-11 shows that the worst case timing for the TM990/E150 module could be satisfied by the use of Schottky devices. For the speed calculation the various delay times of the devices are summed and compared to the requirements of the TM990/E150 MC-module. The result of the comparison shows that the timing requires an optimized circuit design and the use of Schottky devices.

4.5 MEMORY MAPPED INTERFACE

Some highly complex input/output devices such as, for example, the TMS9909 FLOPPY DISC CONTROLLER or the TMS9914 IEEE-BUS CONTROLLER are controlled in a MEMORY MAPPED MODE. The interface of a memory mapped device to E-BUS corresponds roughly to the memory interface previously described. Data and control commands are transmitted on the data bus to different registers on the input/output devices which are addressed using the four lowest order address lines.

Since the address space required by such devices is significantly smaller than that of a memory module, more addresses must be decoded in order to achieve an optimum utilisation of the address space. In E-Systems the memory block >0F000 to >0FFFE is reserved for memory mapped I/O modules and internal microprocessor functions.

4.5.1 CHARACTERISTICS OF MEMORY MAPPED CONTROL

The characteristics of a memory mapped interface are illustrated using the TM990/E353 IEC-module as an example (fig.4-12).

Address bits A0 - A10, as well as the extended address lines XA0 - XA3, are decoded to enable the start address to be relocated in 32 byte steps.

The TMS9914 requires no synchronisation of the bus signals and the BOARD ENABLE controls directly the CE-input.

The READY- lines are driven by a similar circuit as on MEM-modules (see fig.4-10).

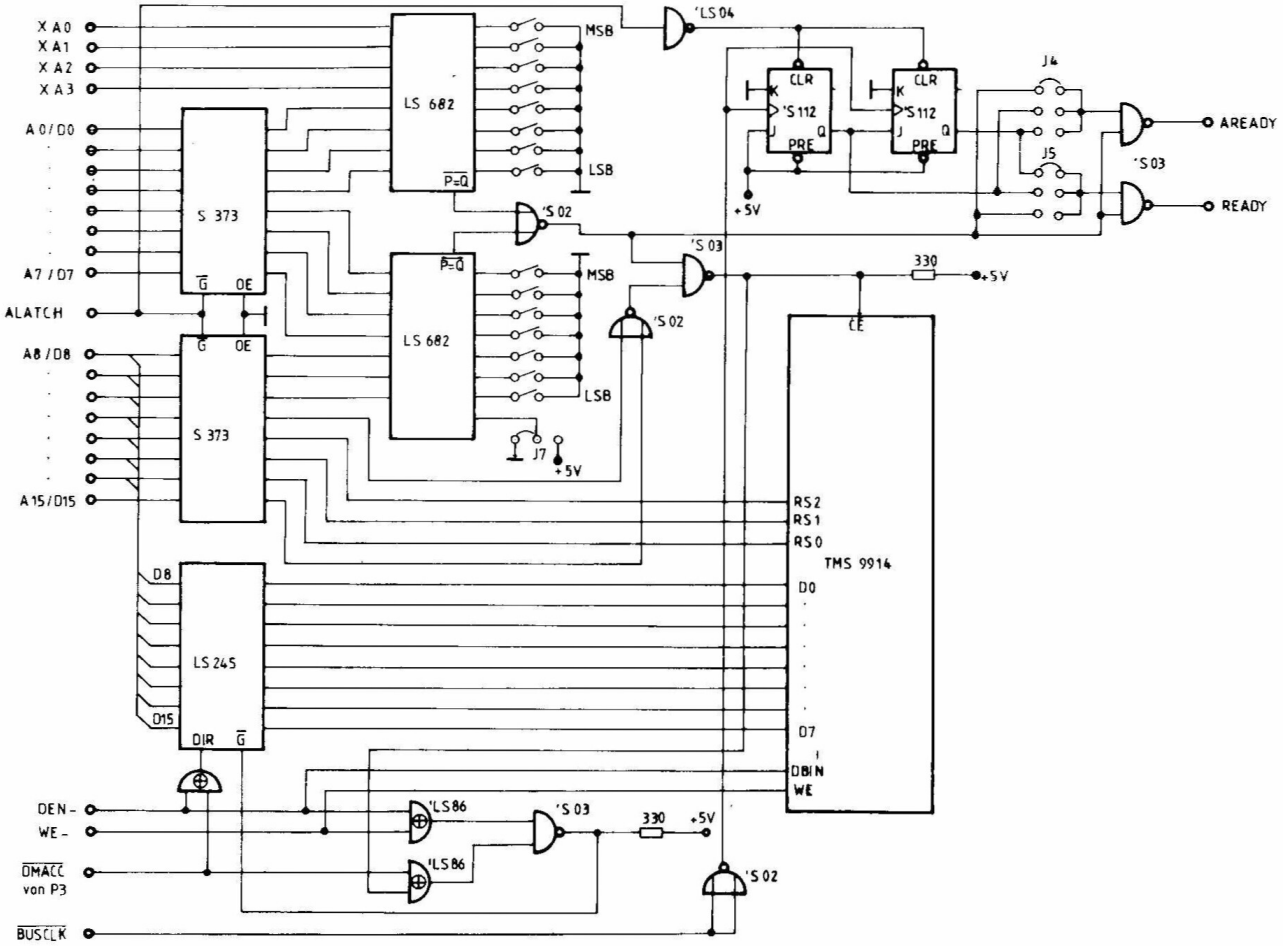


Figure 4-12 TM990/E353 IEC-Module E-BUS Interface

4.5.2 DECODING OF A15 AND MEMWIDTH

E-Bus permits use of processors with either an 8 or a 16 bit wide data bus. The MEMWIDTH signal, produced by the current bus master, informs slave modules of the current width of the data path. MEMWIDTH=HIGH indicates an 8-bit data transfer on lines AD8-AD15. MEMWIDTH=LOW indicates a 16-bit data transfer using all 16 ADI lines.

Byte oriented parallel I/O modules which are to be used with both 8 and 16 bit data paths must use only odd addressed bytes (A15=HIGH) to transfer information. This ensures compatibility with both types of processor.

For byte transfers (MEMWIDTH=HIGH), CE must be generated only when A15=HIGH. The odd byte will then be present on AD8-

AD15. However, a READY- signal must be generated without CE when the module is addressed with A15=LOW, to prevent the processor hanging up the bus if two sequential bytes are transferred as the result of a word instruction.

For word transfers (MEMWIDTH=LOW) A15 should be ignored, as the whole word is transferred at once with A15=LOW. The odd byte will then be available on AD8-AD15, as before.

The alternative to only using odd bytes for 8/16 bit data transfer is to provide a full 8/16 bit memory interface, as described in section 4.6.

An example of parallel input/output via memory mapped I/O is shown in section 7.4.

4.6 8/16 BIT DATA BUS INTERFACE

Using the MEMWIDTH signal it is possible to produce a memory module which communicates by a 16 bit data bus as well as by an 8 bit data bus. When using the 8 bit data bus the transmission of data occurs in two memory cycles via bus lines AD8 - AD15. If the 16 bit data bus is used then the transmission of data is carried out in one memory cycle using the 16 address/data lines. In order to produce a module which can support both the 8 bit bus and the 16 bit bus, a memory architecture must be established having a 16 bit wide memory array which is split into two 8 bit data words. For the parallel 16 bit operation data is presented via two parallelled drivers to the 16 bit bus.

For serial 8-bit operation, all data transmission occurs over the ADI bus lines AD8 - AD15. The 8 highest order data bits are obtained via a third driver connected to the MSB RAM block while the lowest order bits use the LSB data driver to communicate with the LSB RAM block (fig.4-13). A WE- signal must be produced for each RAM block. If in 8 bit mode only one WE- signal were fed to the whole memory block, the MSB and LSB blocks would be written to in parallel and hence correct information would be overwritten on the second write cycle. MEM-Modules to be used with future MC or MMC-modules must support both 8 and 16 bit memory widths.

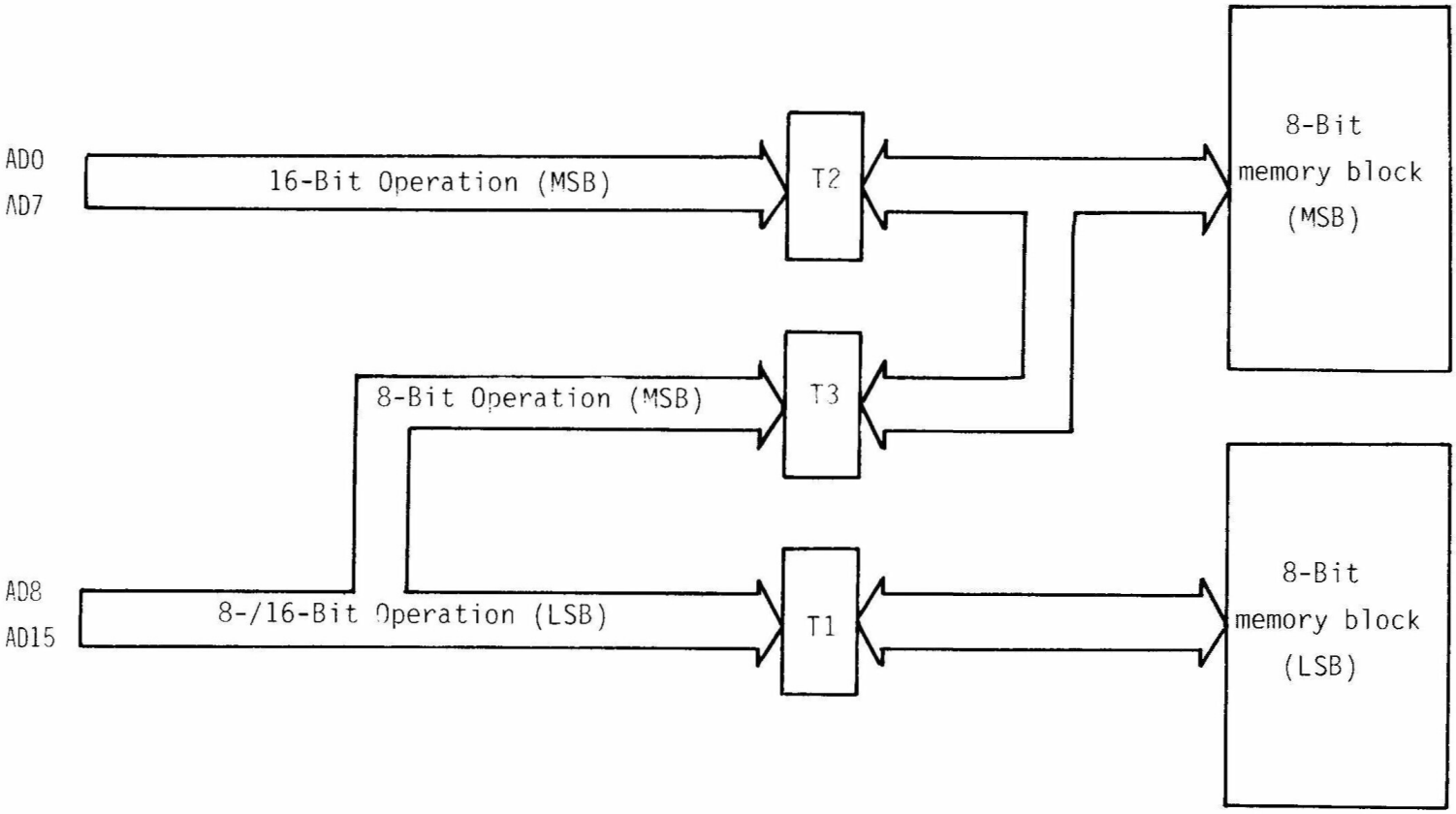


Figure 4-13 Data Flow on the 8/16 Bit Data Bus

4.6.1 CONTROL OF THE DATA DRIVER

The A15 and MEMWIDTH signals control the three data drivers and the two WE lines. This is defined in the following truth table.

A15	MEMWIDTH	T1	T2	T3	WE1	WE2
LOW	LOW	ON	ON	OFF	ON	ON
HIGH	LOW	ON	ON	OFF	ON	ON
LOW	HIGH	OFF	OFF	ON	ON	OFF
HIGH	HIGH	ON	OFF	OFF	OFF	ON

WE1 = WE - MSB RAM Block
WE2 = WE - LSB RAM Block
T1 = Driver - LSB
T2 = Driver - MSB, parallel operation
T3 = Driver - MSB, serial operation

MSB = MOST SIGNIFICANT BYTE
LSB = LEAST SIGNIFICANT BYTE

Fig.4-14 shows the control of the data driver while fig.4-15 shows the complete data bus interface for 8 and 16 bit operation.

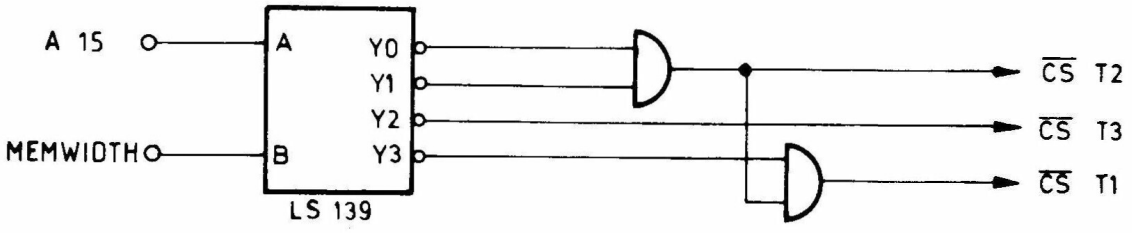


Figure 4-14 Control of the Data Driver

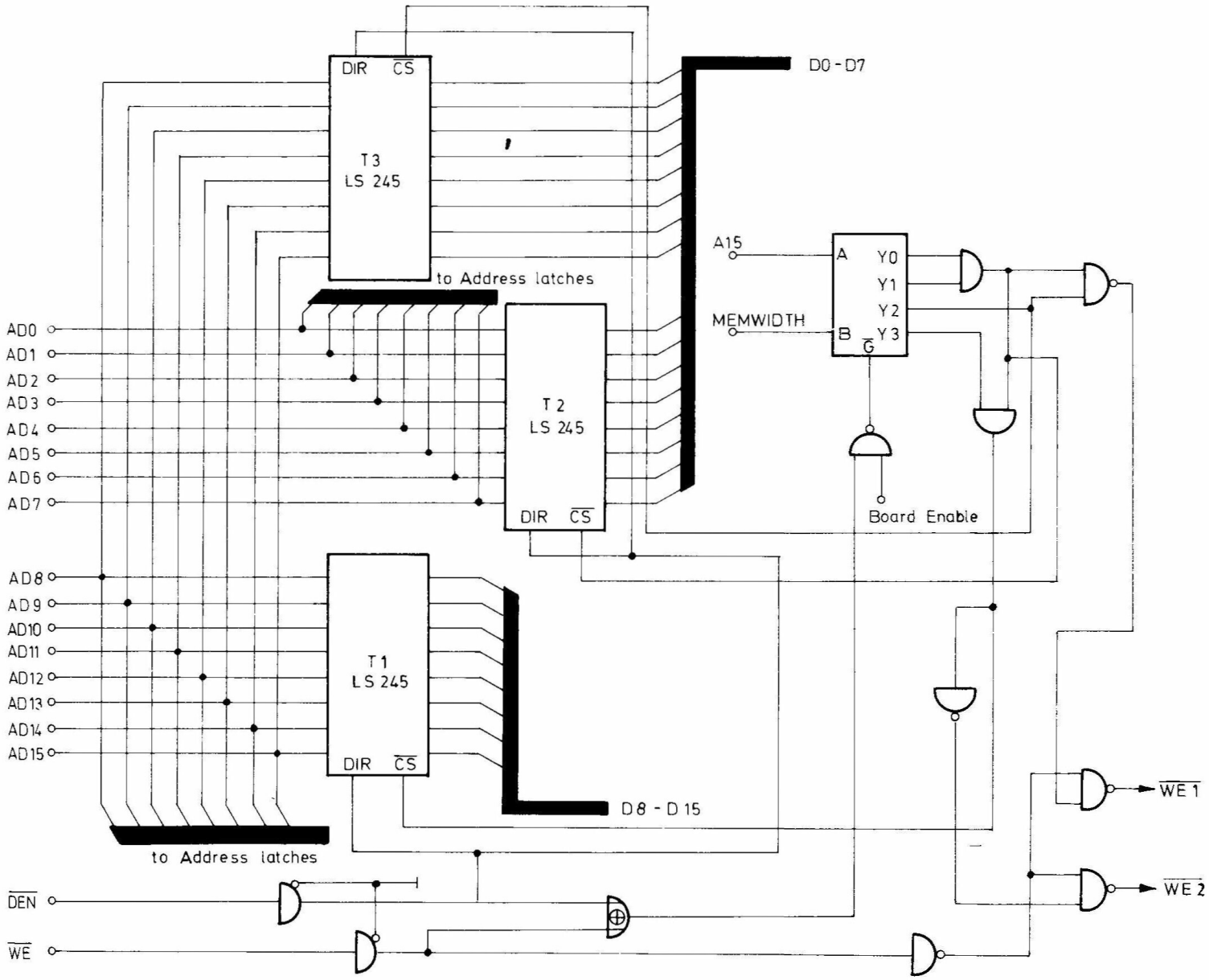


Figure 4-15 8/16 Bit Data Bus Interface

4.7 BATTERY BACKUP

In order to retain data in RAM even on mains failure the memory devices can be supplied from a battery during such an event. E-BUS contains two signals (PRES- and PWRFAIL-) which facilitate the production of memory modules with battery backup. These signals originate from the mains supply and the timings given below correspond to the E-Bus

specification.

The PWRFAIL- signal becomes active 20ms before one of the supply voltages falls out of its nominal tolerance band and is included on the TM990/E150 and TM990/E155 MC-module as a maskable interrupt (interrupt level 1). PRES- becomes active before one of the system supplies falls out of its nominal tolerance band.

This line is used on the memory module to switch supply from the mains to battery backup and also to interrupt the control lines WE- and CS- which must go to the inactive HIGH level.

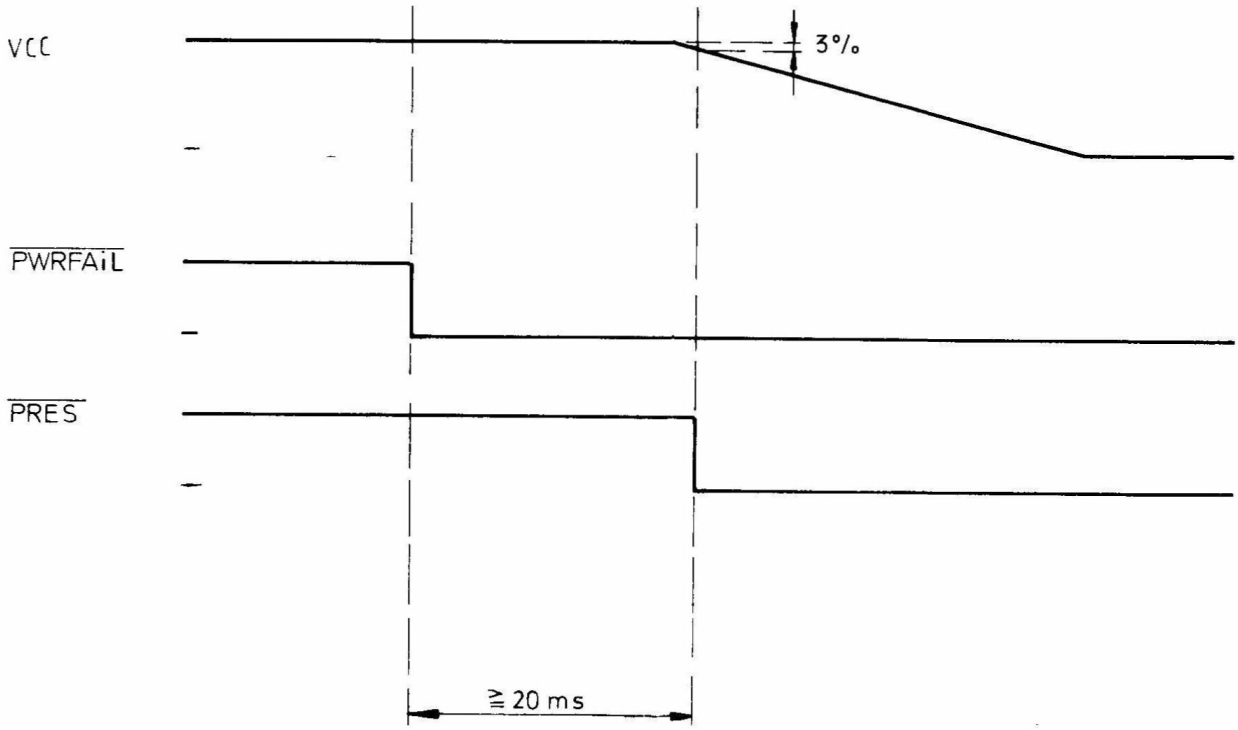


Figure 4-16 Basic Timing Diagram of PRES- and PWRFAIL-

4.7.1 BATTERY BACKUP REALISATION

The following points should be particularly noted regarding the RAM memory battery backup circuitry shown in fig.4-17.

1. The transistor T1 should be selected to have as low a saturation voltage as possible.

2. The buffer for the PRES- signal (T4, T5) must ensure that during the drop in supply voltage to

battery backup conditions, a guaranteed LOW level is maintained for the buffered PRES- signal (collector of T4).

3. The purpose of the diode D1 in the signal path of the control lines is to improve the rise time of the WE- and CS- signals.

4. The battery should be rechargeable and supply a voltage sufficient to counteract the drop produced by the diode. It is recommended that NICAD batteries are used since these have a relatively small volume and are available in hermetically sealed cases.

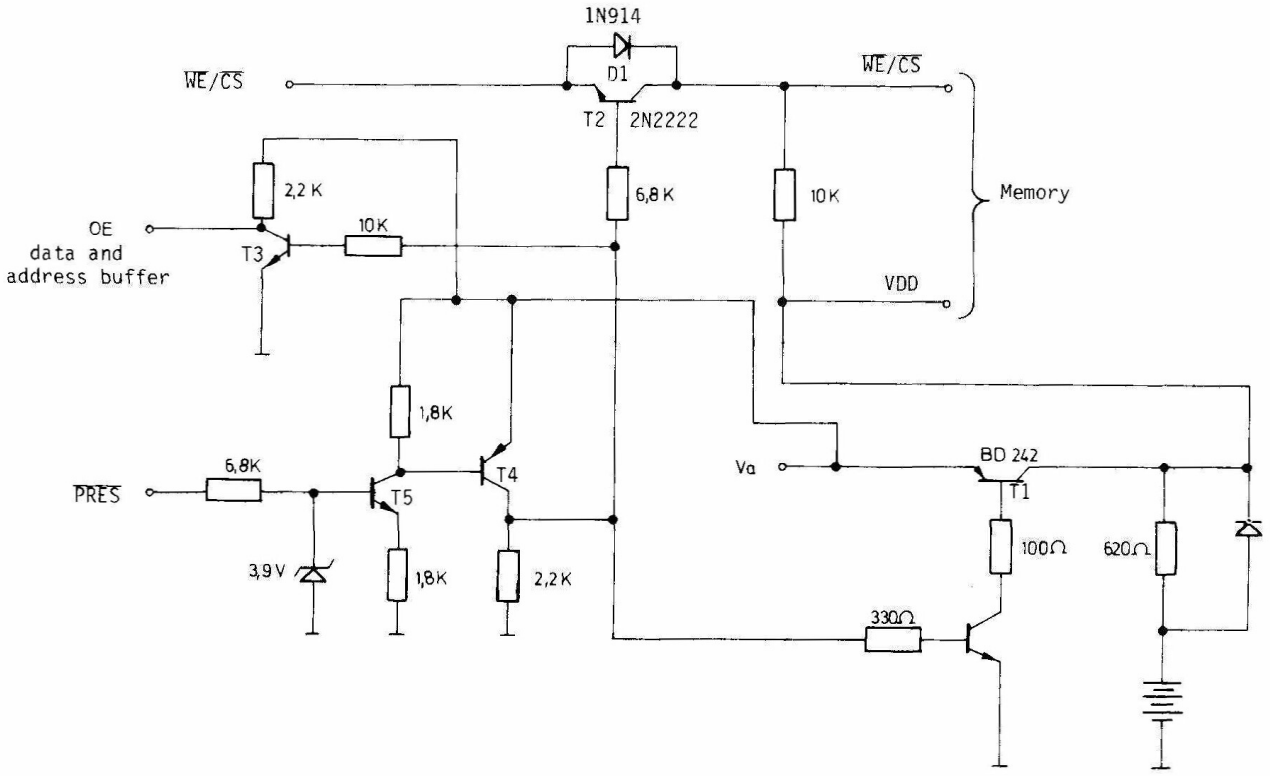


Figure 4-17 Battery Backup

SECTION 5

CRU INTERFACE

The E-BUS supports the bit-oriented CRU interface of the 99XXX microprocessors and the 990 mini computer family (CRU = Communications Register Unit). Compared with a memory mapped I/O interface, this interface offers the following advantages:

- no impact on normal memory space
- variable data format from 1 to 16 bits
- simple single bit input/output/test
- simple interface circuits

5.1 E-BUS CRU SIGNALS

The bit serial CRU interface operates via the signals CRUIN, CRUOUT and CRUCLK-. Addressing of the input/output bits is achieved using the multiplexed ADI bus.

5.1.1 CRU ADDRESS

Up to 4096 (4k) CRU input/output bits may be addressed using the A3/D3/INT3 to A14/D14 lines of the ADI bus. The A0/D0/INT0 to A2/D2/INT2 lines are held LOW during a serial CRU input/output. Using the TMS9900 and TMS9980A/9981 microprocessors, the RESET, IDLE and CLKON commands are transmitted over the highest value CRU address bits. On CRU modules address bits A0 to A2 need not be decoded, since the CRU range of the E-BUS is defined for 4096 input and 4096 output bits.

5.1.2 CRUIN

A MC- or MMC-module reads the input bits, addressed via the address bits A3 to A14, serially via the CRUIN line. On E-BUS CRUIN is a "3-STATE" or "OPEN COLLECTOR" line with a low level drive capability of at least 16mA.

5.1.3 CRUOUT

CRUOUT is the data output line for the bit serial 9900/990 interface and is implemented on E-BUS using the A15/D15 line. Only a processor module which has mastery of the bus may control the CRUOUT and CRUCLK- lines.

5.1.4 CRUCLK-

CRUCLK- (CRU clock) is a "strobe" signal for the serial CRU interface and is active LOW (see fig.5-6) only during a CRU output command (LDCR, SBO, SBZ). CRU modules only accept serial data via the CRUOUT line during the LOW state of, or on the positive edge of CRUCLK-.

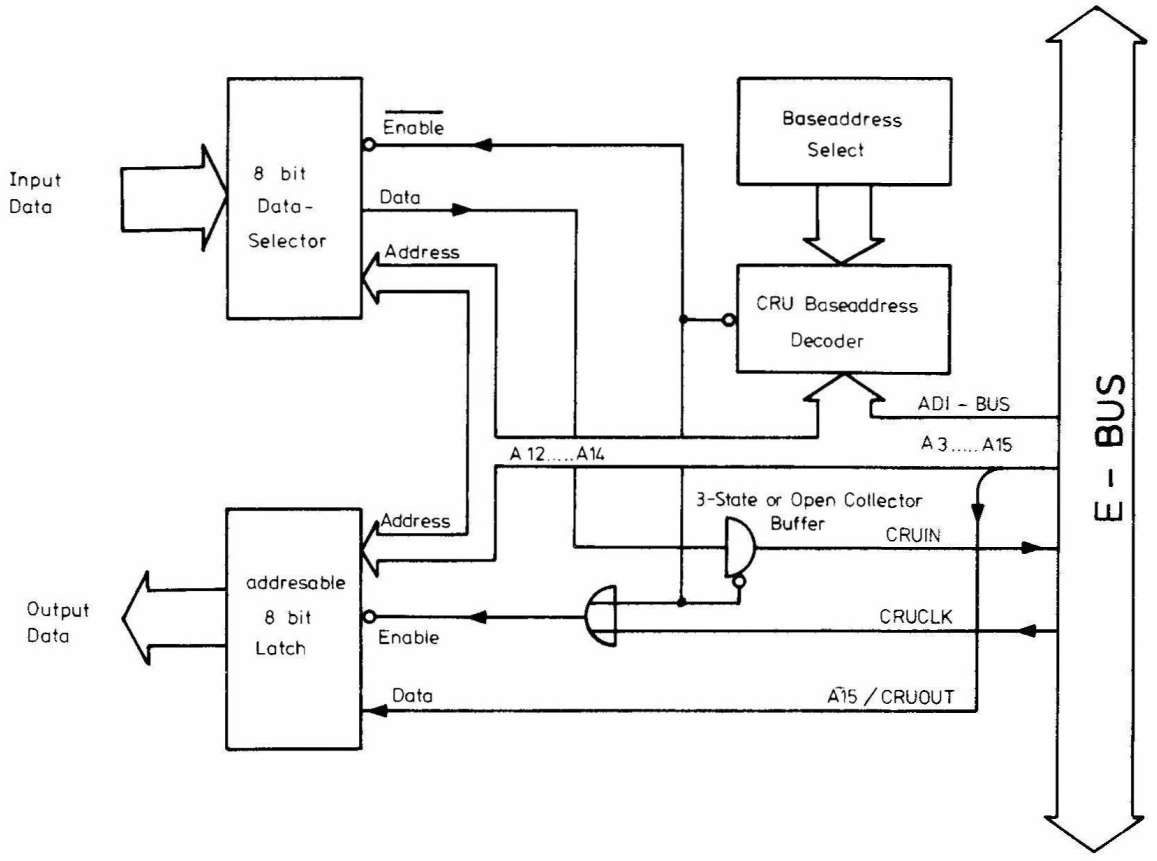


Figure 5-1 CRU Interface Block Diagram

5.2 CRU ADDRESSING

The CRU interface uses the same address lines of the ADI bus as are used for a simple memory interface. However, when used with the serial CRU interface, the ADI bus is used as a static address bus. It is therefore not necessary to store the addresses in some form of memory. The E-BUS control line MEMEN- is used to differentiate between a memory and a CRU address and is only active (LOW) during a memory cycle (see also chapter 4). A CRU module only accepts data in conjunction with CRUCLK- hence, strictly, the state of the MEMEN- line need not be monitored. The CRUIN signal must only be enabled by a select signal from the address decoder of that particular module. The address ranges of different CRU modules must not overlap since a conflict on the CRUIN line could result. When using an E-BUS CRU interface it must be remembered that the address decoder of the CRU module will generate a select signal when the correct bit pattern occurs on the multiplexed ADI bus even if this is due to a similar memory address, data or even an interrupt code. However, since the 9900 microprocessors only interrogate the CRUIN line or generate CRUCLK- during a true CRU cycle, suppression of such a false CRU cycle is not required.

5.2.1 CRU BASE ADDRESS

A typical CRU module occupies 8, 16, 32 or 64 bits of the CRU range, however a general division into 32 bit blocks is recommended. The direct addressing of a particular input/output bit occurs using the 3 to 6 lowest order CRU address bits (...A14) while the highest order address bits (A3...) form the "base address" of a CRU module (see table 5-1). The address decoder generates the select signal for the module input/output circuitry using these highest order bits.

Number of Ports	8 bit	16 bit	32 bit	64 bit
I/O Select	A12...A14	A11...A14	A10...A14	A9...A14
Base Address	A3...A11	A3...A10	A3...A9	A3...A8

Table 5-1 Address Bits for CRU Decoding

NOTE

On a CRU module all higher value address bits (up to A3) should be decoded to

allow for expansion of an existing system at a later date.

5.2.2 DEFINITION OF THE CRU BASE ADDRESS

The CRU commands (SBO, SBZ, TB, LDCR and STCR) operate using relative addressing with register R12 acting as an index register, containing the so-called base address. In the 9900 literature (see also Software Development Handbook) the terms SOFTWARE and HARDWARE base address are used and hence the following definitions are included to explain the differences in detail:

Software base address

Register R12 contains the base address in bits 3 to 14 (bits 4 to 14 for TMS9980A/9981) for CRU addressing. If the remaining bits are set to 0 then the value of the contents of R12 is equal to the software base address.

Hardware base address

The hardware base address is equal to the value stored in R12 with bit 15 omitted. It is therefore half the corresponding software base address. The hardware base address has the advantage that it provides direct information of the absolute address of the CRU bit.

NOTE

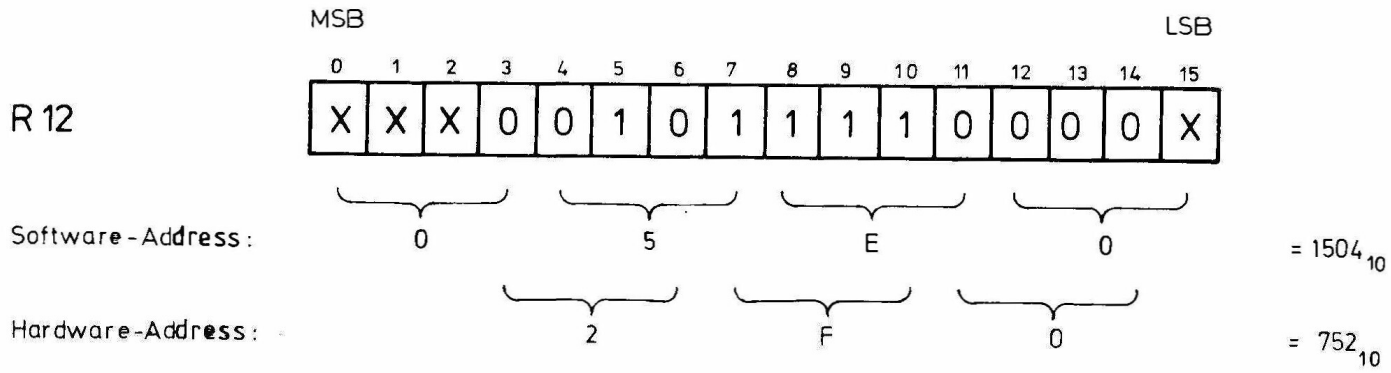
To avoid confusion only one of these two addresses should be used. In practice it has proved advantageous to use only the software base address.

5.2.3 CRU ADDRESSING EXAMPLE

The example below illustrates the relationship between the software and hardware addresses as well as the addressing of a particular CRU bit (called here PORTN). From this example it can be seen that the fact that the CRU signals are being communicated over the multiplexed E-BUS does not affect the way the CRU interface program is written.

```
Address  Code  Label  Mnemonics  Operand     Comment
         05E0  BASE   EQU        1504        CRU BASE ADDRESS
         FFED  PORTN  EQU        -19         OUTPUT PORT N
               *
               *
  0A0E  020C          LI         R12,BASE    LOAD CRU BASE ADDRESS
  0A10  05E0
  0A12  1DED          SBO        PORTN       SET PORT N
```

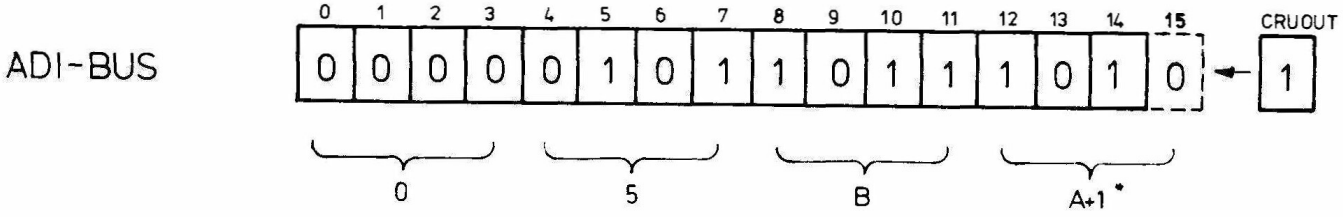
After the above sequence has been performed R12 contains the following value:



The address on the ADI bus is equal to the base address plus the relative address (in this example -19 = >FFED).

Bus address = 1504 + 2(-19) = 1466
= >05E0 + >FFDA = >05BA

During the execution of the above SBO command the E-BUS is in the following state:



Bit 15 (CRUOUT) is HIGH as a result of the SBO command (SBO = set bit to one).

5.3 CHOICE OF CRU BASE ADDRESS

5.3.1 RESERVED CRU ADDRESSES IN THE E-SYSTEM

To achieve software compatibility between different TM990/E systems, certain ranges of the CRU address space are reserved for special functions.

Table 5-2 shows that the address range >400 to >7FE (contents of R12 = software base address) is available for general applications, while the range 0 to >3FE is reserved for applications relating to the MC- or MMC-module. The address range from >800 to >1FFE is reserved for common and private I/O-units on the E-Bus, CRU expansion chassis and on-chip functions of the 99XXX micro-processors.

Software Address	Typical Function
0 - >3E	System status flags
>40 - >5E	System configuration switch
>60 - >6E	Memory mapping control bits
>70 - >7E	Reserved
>80 - >BE	Terminal interface (prim.port)
>C0 - >FE	Reserved
>100 - >13E	Timer, interrupt control bits
>140 - >17E	Reserved
>180 - >1FE	Terminal interface (sec.port)
>200 - >3FE	Reserved
>400 - >7FE	User CRU, freely available
>800 - >1FFE	Reserved

Table 5-2 TM990 CRU Address Mapping

5.3.2 TM990/E150 MODULE CRU ADDRESS MAP

When developing a system with E-BUS, a knowledge of the processor module CRU address mapping is essential. Table 5-3 below shows as an example the CRU address mapping of the TM990/E150 processor module. The range >200 to >FFE (R12) is available to the user for specific expansions. The range

>180 to >1FE should only be used when there is only one terminal interface (see Table 5-2).

The CRU range >1000 to >1FFE (R12) is not addressed with the TM990/E150 module since the TMS9981, as used on this module, only addresses a 2k bit (2048) range with its 11 CRU address bits. The TMS9981 microprocessor ignores bits 0 to 3 of register R12 and sets the E-BUS address lines A0 to A3 LOW during a CRU operation.

NOTE

The lowest value TMS9981 address bit A13/CRUOUT corresponds to address bit A15/CRUOUT on E-BUS.

Hardware Address	Software Address	Function
0 - >1F	0 - >3E	32 bit flag register (on board)
>20 - >3F	>40 - >7E	32 bit external CRU
>40 - >5F	>80 - >BE	32 bit serial I/O port TMS9902
>60 - >9F	>C0 - >13E	64 bit external CRU
>A0 - >BF	>140 - >17E	PWRFAIL- line test (Pin 24a)
>C0 - >3FF	>180 - >7FE	832 bit external CRU
>400 - >7FF	>800 - >FFE	1k bit flag register (on board)

Table 5-3 TM990/E150 CRU Address Mapping

5.4 ADDRESS DECODER SELECTION CRITERIA

On a CRU module, base address decoding can be performed with either combinational logic, a PROM or a comparator. Table 5-4 gives the most relevant data relating to four custom address decoders. Typical advantages and disadvantages of these three approaches are explained below.

Address Decoder	Bus Load**		Delay Time
	UBL(low)	UBL(high)	tD
Combinational Logic *	2	1	<35ns
PROM (TBP14S10)	1.25	1.25	<65ns
Comparator (SN74LS266)	4	2	<30ns
Comparator (SN74LS682)	1	1	<25ns

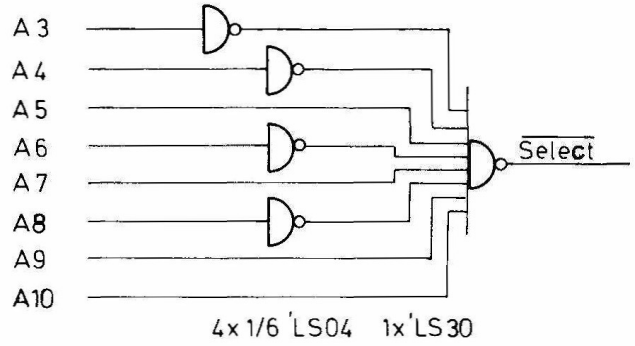
* see fig.5-2 ** see section 2.5.2

Table 5-4: Typical Data for Different Address Decoders

5.4.1 COMBINATIONAL LOGIC

Combinational logic is normally only used for specific applications, i.e. within microcomputer systems where the configuration will remain static for all time.

Chapter 7 gives an example of a serial system interface relating to the application of the TMS9902/3. The address range >180 to >1FE is reserved for a terminal interface corresponding to the TM990/E CRU address map (see table 5-2).



CRU-Base address: > 560 (R12)

Bus-Load : $I_{IL} \geq -400\mu A$
Delay time: $t_{PHL} \leq 35\,ns$

Figure 5-2 Fast Combinational Logic CRU Address Decoder

5.4.2 COMPARATOR WITH DIL SWITCHES

In practice a comparator with DIL switches or jumpers is most frequently used for address decoding as it offers many advantages, particularly during the development phase of a system. A suitable circuit can be constructed relatively simply using the SN74LS682 8 bit comparator which has integrated pull up resistors on the Q inputs. An 8 bit address decoder constructed using the 'LS682 consists (in contrast to that shown in fig.5-3) of only two components (see also fig.5-7).

At this point the possibility of decreased reliability must be mentioned: DIL switches, while being very cost effective, can suffer from contact oxidisation caused by the ingress of foreign material. This may result in the incorrect decoding of a LOW address bit.

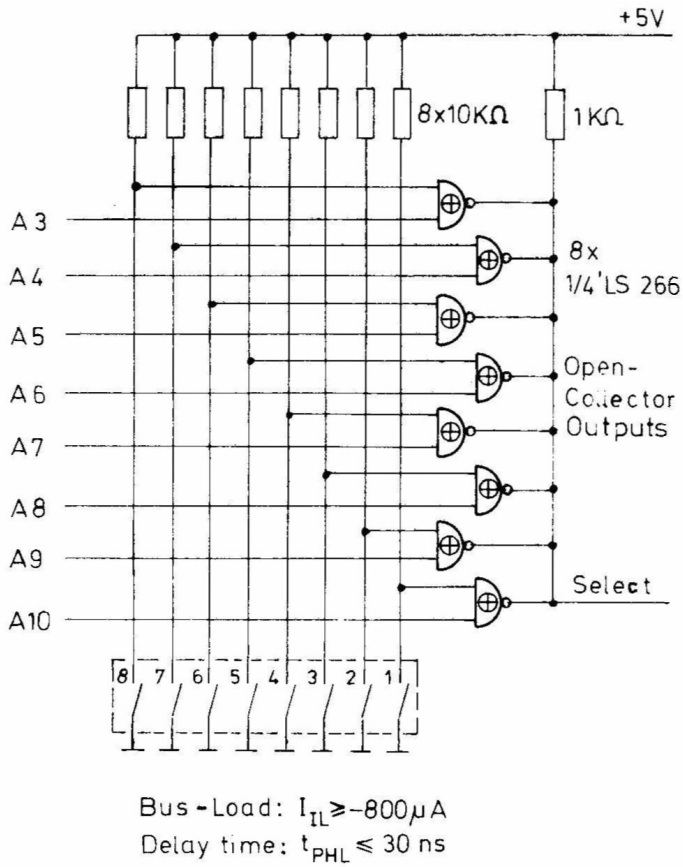
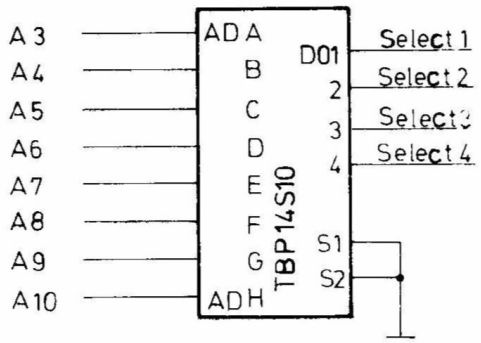


Figure 5-3 Comparator with DIL Switches

5.4.3 PROM

A PROM enables the simultaneous decoding of several address ranges on a complex CRU module (also applicable to both CRU and memory addresses). It offers the further advantage of relatively small physical space requirements (only one IC) and also offers individual programming since PROMs may be easily interchanged provided they are socketed.



Bus-load : $I_{IL} \geq -250\mu A$
Acces time: $t_a \leq 65ns$

Figure 5-4 PROM as CRU Address Decoder

5.5 CRU INTERFACE TIMING REQUIREMENTS

Fig.5-5 and table 5-5 show the timing requirements for the CRU interface of the E-BUS (BUSCLK- = 2.5 and 3MHz).

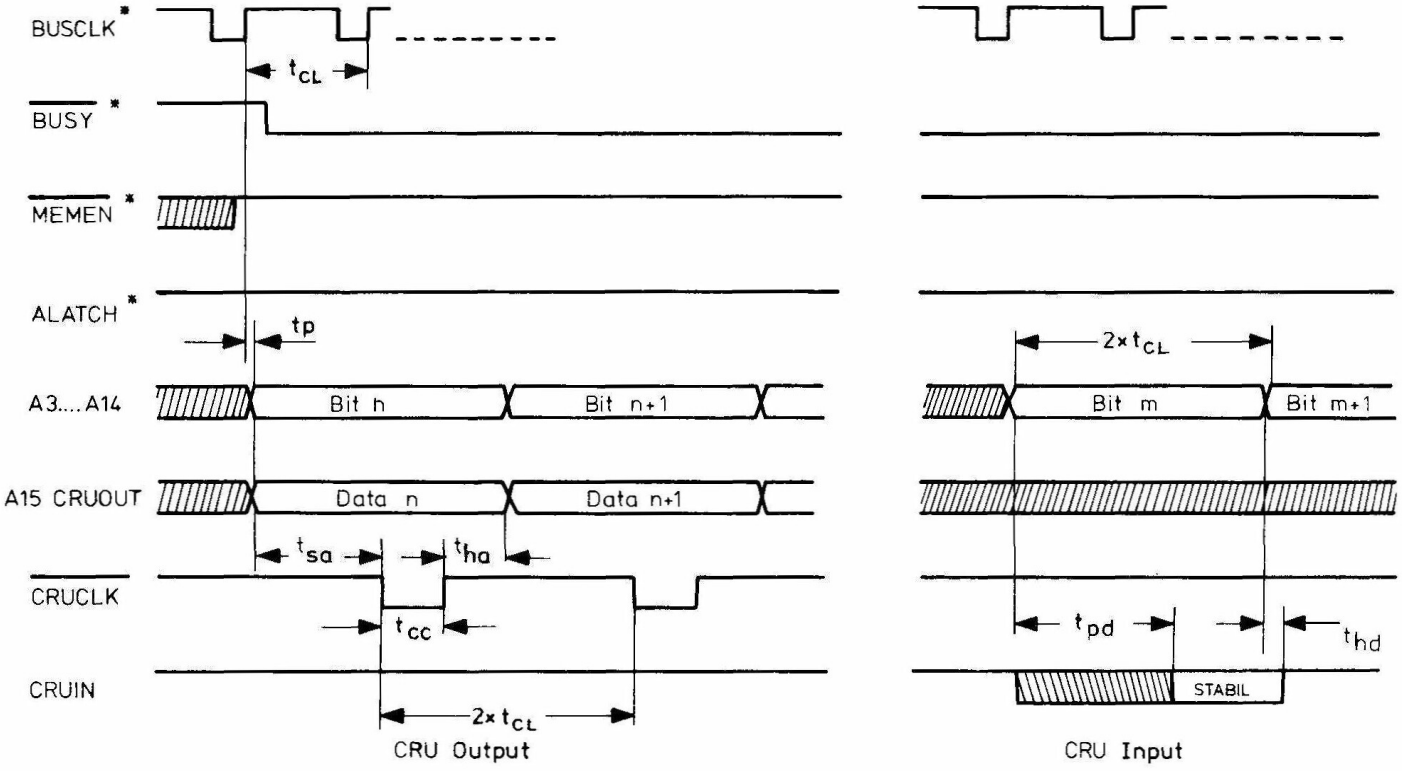


Figure 5-5 CRU Timing Diagram

PARAMETER	2.5MHz	3.0MHz
clock cycle time	tcl >400 ns	tcl >333 ns
pulse width CRUCLK- low	tcc >160 ns	tcc >130 ns
setup time before CRUCLK-	tsa >190 ns	tsa >250 ns
hold time after CRUCLK-	tha >180 ns	tha >100 ns
propagation delay from address	tpd <470 ns	tpd <400 ns
hold time after address	tdh > 10 ns	tdh > 10 ns
propagation delay from BUSCLK- high	0ns<tp< 50 ns	0ns<tp<50 ns
setup time, BUSY, before BUSCLK- high	tsb > 30 ns	tsb > 30 ns
setup time before CRUCLK-	tsc > 30 ns	tsc > 30 ns

Table 5-5 CRU Timing Requirements

5.6 EXAMPLE OF A CRU OPERATION

Fig.5-6 shows an example of the operation of the CRU interface, illustrated using the LDCR command. In this program sequence register R12 is first loaded with the CRU base address while register R4 is loaded with the outgoing bit pattern 101 (=5).

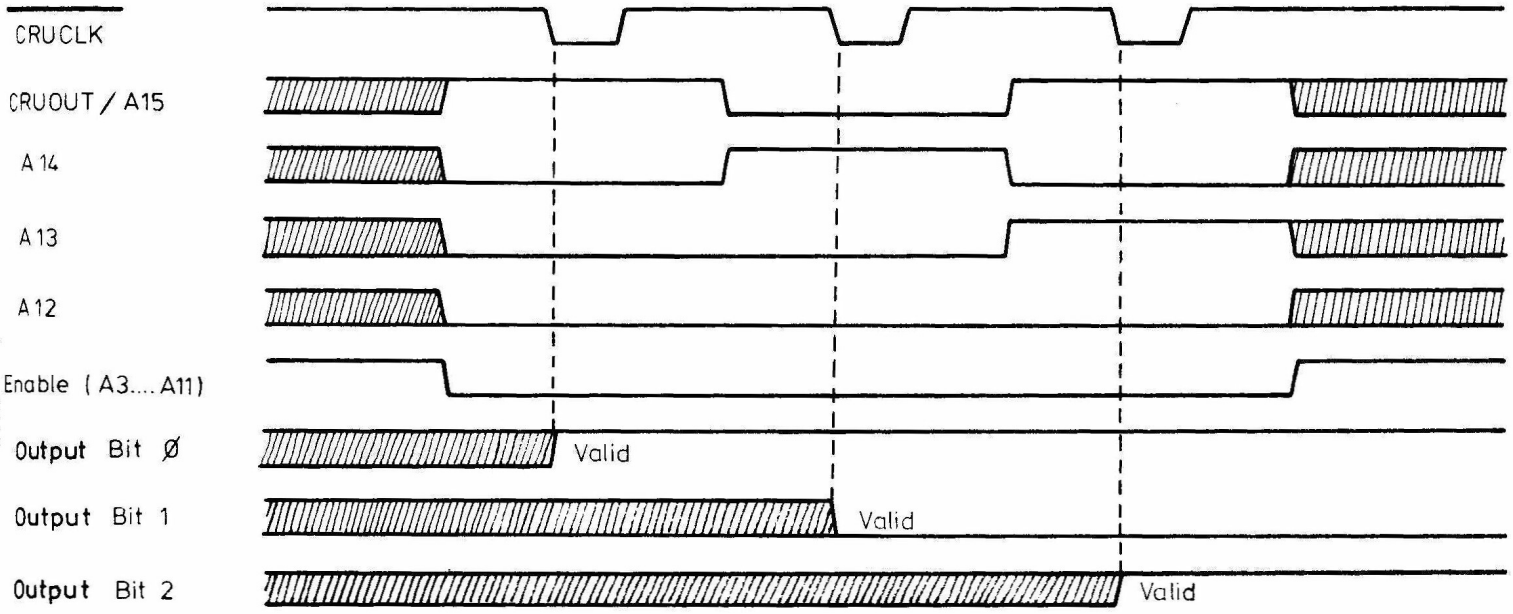


Figure 5-6 3 Bit CRU Operation

Programming example:

```
Address Code  Mnemonics  Operand     Comment
  13D8  020C  LI         R12,>400    LOAD CRU-BASE ADDRESS
  13DA  0400
  13DC  0204  LI         R4,>500     LOAD OUTPUT VALUE
  13DE  0500
  13E0  30C4  LDCR       R4,3        LOAD 3 CRU BITS
```

After this sequence has been performed register R4 contains the value 5 in the left byte. Assuming the CRU interface shown in fig.5-7 the following connection between the contents of register R4 and the circuit shown applies:

```
Register bit 7 = Output bit 0 (LSB)
Register bit 6 = Output bit 1
Register bit 5 = Output bit 2 (MSB)
```

In the module shown in fig.5-7 the base address >400 (R12) is set up as shown: S3 of the DIL switch is in the OFF position (OFF = HIGH), all other contacts are in the ON position.

If a TM990/E150 processor module is used in the previous example (2.5MHz system clock) then the time difference between the output (or input) of two bits (2 x tc1 in fig.5-5) is typically 800ns.

5.6.1 EXAMPLE OF A CRU INTERFACE

The CRU interface shown in fig.5-7 illustrates the relatively low number of components which are required for a parallel 16 bit input/output interface to E-BUS.

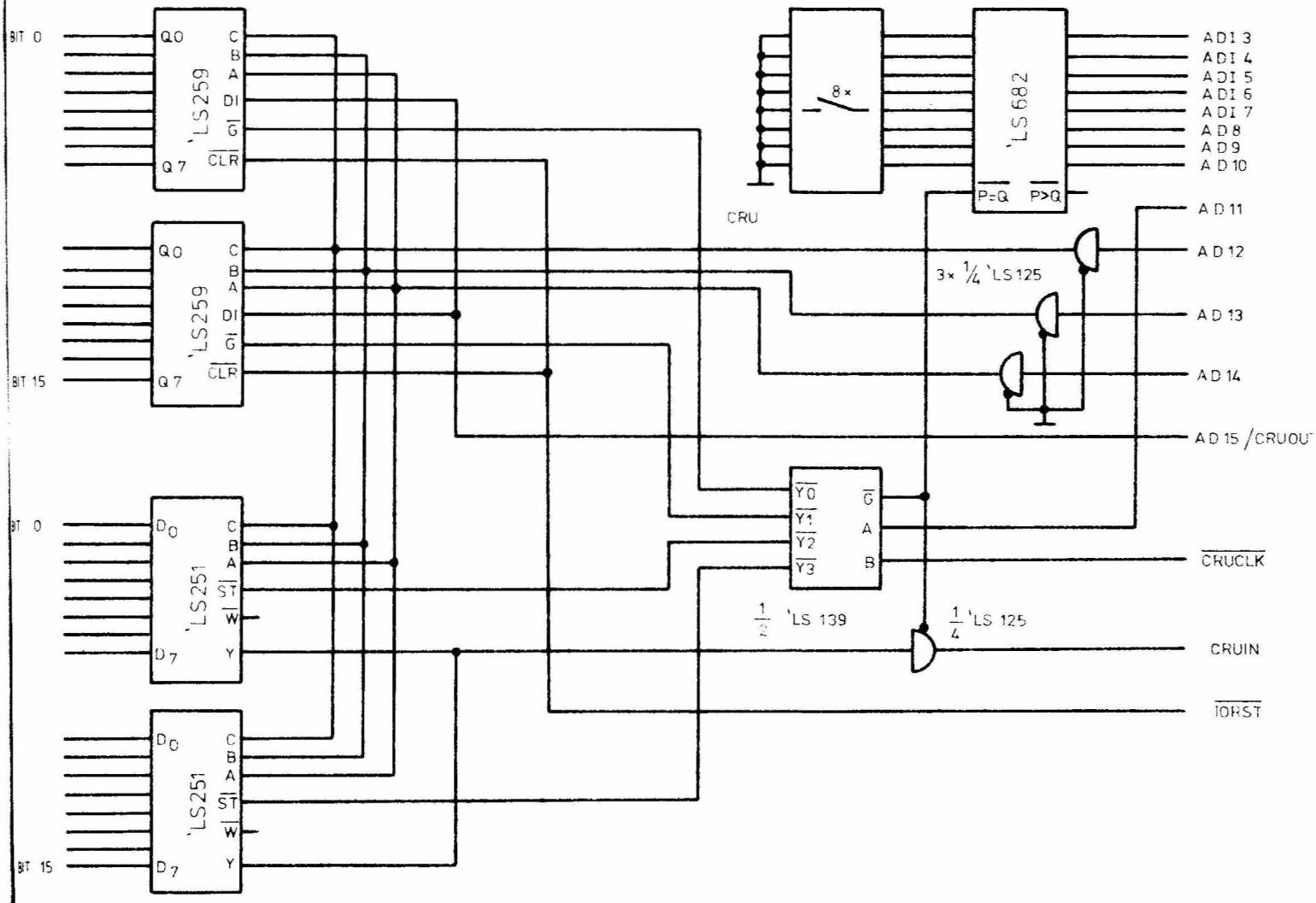


Figure 5-7 16 Bit CRU Input and Output Interface

The circuit example uses the ´LS259 addressable latches for the output and ´LS251 data selectors for the input. The three ´LS125 drivers are used to minimise the fan in of the bus signals AD12 to AD14. The fourth ´LS125 driver increases the drive capability of the CRUIN signal to that recommended in the E-BUS electrical specification (see also chapter 2). This 3-STATE driver can also be used in an OPEN COLLECTOR mode by exchanging the signal input with the enable input. An additional PULL UP resistor at the Y outputs of the ´LS251 is however required.

Further CRU interface circuit examples are shown in chapter 7.

SECTION 6

INTERRUPT OPERATION

The E-BUS vectored interrupt system has multiprocessor capability and utilises a 7 bit interrupt code. The transmission of this code occurs over the multiplexed ADI bus.

6.1 STATIC INTERRUPT SIGNALS

As a rule the three static vectored interrupts PRES-, NMI- and PWRFAIL- are assigned the highest priority within a microcomputer system. As each of these three signals has a dedicated static line, all microprocessors within the system can react to these interrupts with a minimum of delay.

PRES-, NMI- and PWRFAIL- can be fed completely asynchronously to the E-BUS using OPEN COLLECTOR gates, i.e. transmission of these interrupts does not require arbitration of the bus (no arbitration logic). As they are OPEN COLLECTOR signals, different interrupt sources may be WIRE-ORed onto the bus. The drive capability of each output should be at least 16mA.

6.1.1 PRES-

PRES- (Power on Reset) is a non-maskable interrupt* which forces a reset of all master and slave modules within the system. PRES- should be maintained at an active LOW by the system mains supply until all supply voltages are stable. In addition PRES- must also go LOW prior to any of the supply voltages leaving its nominal tolerance range. Generally the PRES- signal is produced by additional circuitry within the supply and must go LOW even during a momentary drop in supply voltages. This is necessary since the PRES- signal is used on various battery back-up memory modules to produce the relevant control signals (see also fig. 3-4 and 4-7).

6.1.2 NMI-

NMI- (Non Maskable Interrupt) is a non-maskable interrupt*

* maskable using the microprocessor status register

operating on system MC- or MMC-modules. On the TM990/E150 module this active LOW signal causes an interrupt of the TMS9981 via its LOAD vectors (see table 6-3). Possible sources of the NMI signal are a front panel switch or the WATCH-DOG timer on the TM990/E351 module. With the aid of a jumper the output of this timer may be connected to the E-BUS NMI- line, and thus may become one of the circuits monitoring correct system operation.

6.1.3 PWRFAIL-

PWRFAIL- (Power fail) is a maskable vectored interrupt on E-BUS. This signal being active (LOW) indicates a drop in the mains supply and is produced by suitable logic included in the power supply.

The supply voltages must remain stable for at least 20ms after PWRFAIL- goes active. This period is usually sufficient to enable essential data to be stored in non volatile memory. On the TM990/E150 processor module, the PWRFAIL- interrupt operates using the TMS9981 level one interrupt vectors (see table 6-3).

In LOW COST systems using the TM990/E151 OEM-module the PWRFAIL- line may be used as an interrupt request signal. All interrupt requests are combined on this line and hence utilise the same vector. To ensure that the program branches to the correct service routine, the source of the interrupt must be ascertained using the CRU interface. Suitable additional software control can assign relevant priorities to the sub-programs.

6.2 GENERAL INTERRUPT SIGNALS

Previously bus systems with vectored interrupts (e.g. the T series, T-100-Bus) utilised a static line for each interrupt source. Thus only a limited number of interrupts were realisable, set by the number of lines available, and hence in a multi-microcomputer system partitioning of the interrupts was required. The E-BUS avoids this disadvantage by the use of coded vectored interrupts (interrupt code).

6.2.1 INTERRUPT CODE

Use of the 7 bit interrupt code INT0 to INT6 allows up to 128 different vectored interrupts to be generated within one multi-processor system. Transmission of this code occurs via the 7 lines ADI0 to ADI6 of the 16 bit wide ADI bus, leaving

9 lines unused for possible future expansion of the interrupt code.

Table 6-1 shows that the interrupt code is divided into three bits for processor address and four bits for the coded vectored interrupt. In a multi-processor system the processor address enables the selective transmission of interrupts such that only the microprocessor for which the interrupt is intended is interrupted.

In the simplest case the interrupt code may be produced using a 7 bit DIL switch. Alternatively the code of the interrupt level can be generated using the TMS9901 interface circuit or an SN74LS148 prioritiser and the processor address stored in a special register. This system may be used to produce, say, a DMA-module with multi-processor capability. The register can be loaded by the initialising MMC-module while the end of the data transfer is indicated by an interrupt to the corresponding MMC-module.

A further example of the formation of the interrupt code is given in chapter 7.

INT0	INT1	INT2	Processor	INT3	INT4	INT5	INT6	Level
0	0	0	1	0	0	0	0	0
0	0	1	2	0	0	0	1	1
0	1	0	3	0	0	1	0	2
0	1	1	4	0	0	1	1	3
1	0	0	5	0	1	0	0	4
1	0	1	6	0	1	0	1	5
1	1	0	7	0	1	1	0	6
1	1	1	8	0	1	1	1	7
				1	0	0	0	8
				1	0	0	1	9
				1	0	1	0	10
				1	0	1	1	11
				1	1	0	0	12
				1	1	0	1	13
				1	1	1	0	14
				1	1	1	1	15

Table 6-1 Interrupt Code INT0 to INT6

It can be seen from table 6-1 that the code for level 0 is not used (i.e. no interrupt), but it may be decoded to produce, for example, a selective reset. Via this form of interrupt code E-BUS supports the principle of prioritised interrupt service routines. Interrupt level 1 has the

highest priority, i.e. its interrupt service routine can only be interrupted by a non-maskable interrupt (e.g. PRES-). On the other hand level 15 can be interrupted by all other interrupt levels. However, the exact handling of the different prioritised interrupts can be modified by the interrupt mask loaded into the status register of the microprocessor.

6.2.2 CONTROL SIGNAL INTEN

The signal INTEN- signifies that an interrupt code is being transmitted on the multiplexed ADI bus. This signal is active LOW and is simultaneously switched to the E-BUS together with the interrupt code. As bus signals INT0 to INT6 are 3-STATE signals, a bus arbitration is necessary, controlled by the BUSY-, GRANTIN and GRANTOUT signals.

6.3 INTERRUPT CODE TRANSMISSION

The bus arbitration for the transmission of the interrupt code consists of the following four phases:

1. Interrogate E-BUS
2. Wait until bus is free
3. Switch interrupt code to bus
4. Release E-BUS

The bus arbitration is repeated every 100 BUSCLK- cycles by the interrupt hardware until the relevant service routine has reset the interrupt source.

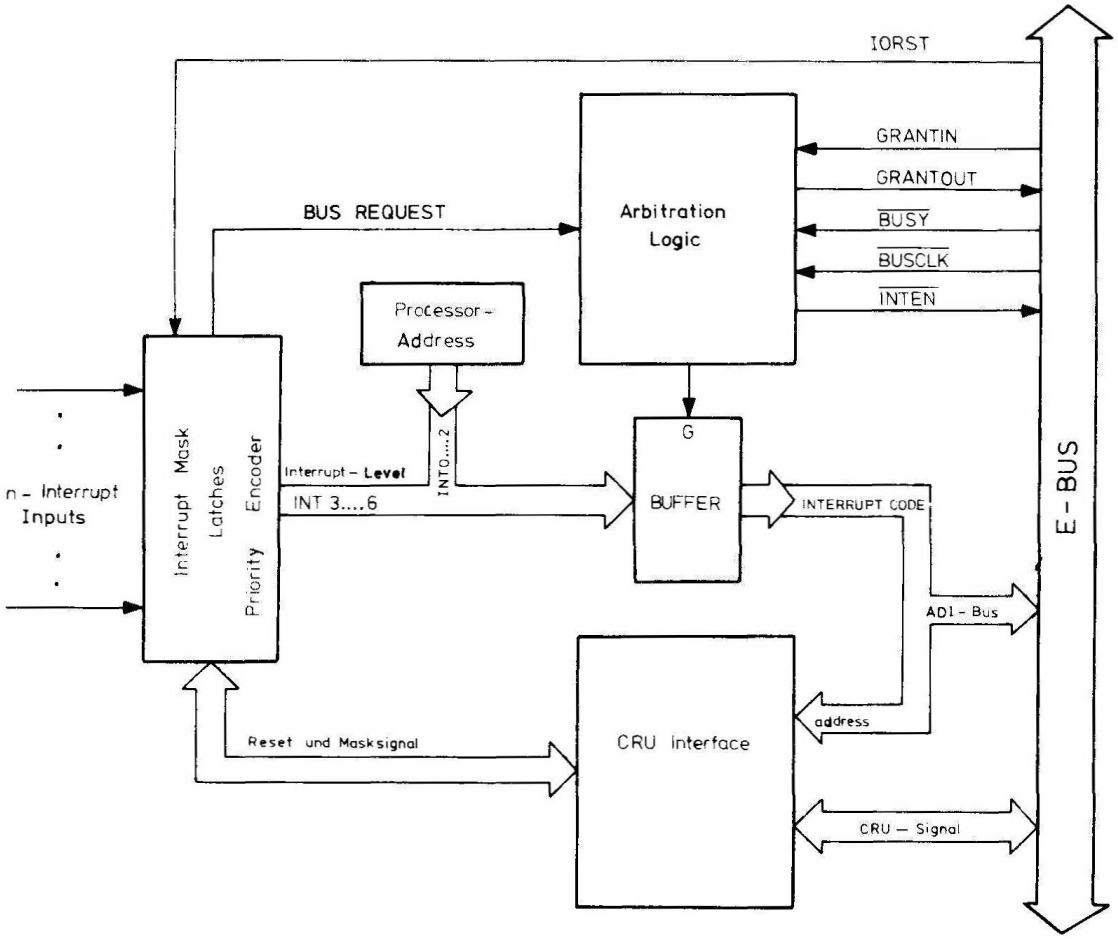


Figure 6-1 Block Circuit Diagram of an Interrupt Module

6.3.1 BUS ARBITRATION

All E-BUS arbitrations are controlled using the GRANT lines in a DAISY-CHAIN fashion. Modules signify that they require the bus by setting their GRANTOUT line LOW. This prevents all modules having lower priority from contending for mastery of the bus - and a lower priority module which may have control of the bus at the time is required to suspend execution and release the bus.

6.3.2 WAIT UNTIL BUS FREE

A module can only acquire the ADI bus when BUSY- and GRANTIN are in the HIGH state. The BUSY- line is active LOW and signifies the current condition of the E-BUS while GRANTIN, when LOW, shows that a module with higher priority is in

control of the bus or has requested the bus.

6.3.3 SWITCHING THE INTERRUPT CODE TO THE BUS

Only when the conditions for arbitration of the bus have been fulfilled (GRANTIN and BUSY- are HIGH) can the interrupt code be switched to the bus on the next positive edge of BUSCLK-. Simultaneously, the INTEN- line is set LOW to indicate to all processor modules the transmission of an interrupt code. The control of the BUSY- line is not required since the duration of this arbitration is only one BUSCLK- cycle and the bus becomes free again with the next positive edge of BUSCLK-.

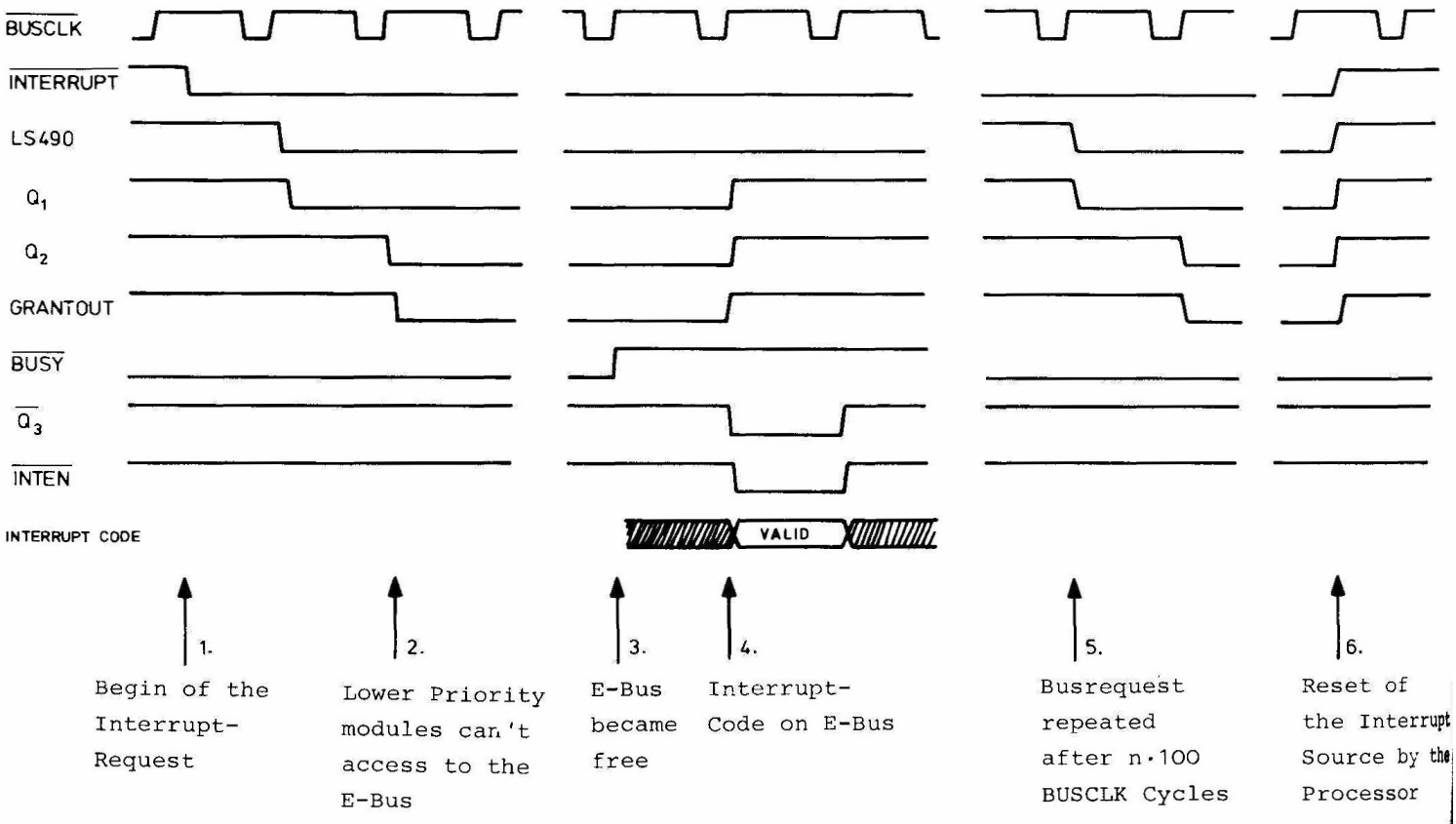


Figure 6-2 Bus Arbitration Cycle

6.3.4 REPETITION OF THE BUS ARBITRATION

The interrupting module must repeat the transmission of the interrupt code until the addressed microprocessor terminates the interrupt request by resetting the interrupt source. This is necessary because:

1. at the time the addressed microprocessor may be servicing a higher priority interrupt. In this case the microprocessor interrupt mask locks out the interrupt level transmitted so that lower priority interrupts are not recognised. The transmitted interrupt request is only stored for the duration of one IAQ cycle* and would be, in this case, lost (see also section 6.5). An interrupt service routine can, however, be interrupted by a higher level interrupt, in which case the new service routine is initiated.

2. during a particular IAQ cycle* two or more interrupt modules can transmit codes to the same processor module. In the case of the TM990/E150 processor module, the logic only stores that interrupt code having the higher priority. Only when the source of this interrupt has been serviced may the lower priority interrupt be stored and serviced.

NOTE

The interrupt code must be repeatedly transmitted until the interrupt source is reset, otherwise a satisfactory response cannot be guaranteed from the processor module.

* During an IAQ cycle the microprocessor executes one instruction and then tests whether a valid interrupt code exists before fetching the next instruction.

6.4 BUS ARBITRATION TIMING

6.4.1 CONTROL OF A BUS ARBITRATION

Fig.6-3 shows a circuit for transmission of the interrupt code (bus arbiter). Operation of the circuit is initiated by the "interrupt request" which by going LOW effectively enables the ´LS490 decade counter and the first flip-flop. The subsequent positive edge of BUSCLK- triggers the first flip-flop via the resulting negative edge at the 2QD output of the decade counter. Unfortunately the resulting signal delay times are not compatible with the E-BUS specification

(see table 6-2), hence synchronisation by the second flip-flop is required. This results in a maximum delay time from the positive edge of BUSCLK- to GRANTOUT going LOW of 19ns. If both GRANTIN and BUSY- are in the HIGH state then the interrupt code and the INTEN- signal are switched to the E-BUS on the next positive edge of BUSCLK-. This is controlled by the third flip-flop and the 'LS244 buffer.

The first and second flip-flops are reset simultaneously together with the GRANTOUT output, and transmission of the interrupt code is concluded with the next positive edge of the BUSCLK-.

The interrupt request signal must remain active until the microprocessor reacts to the interrupt and resets the interrupt source. If this does not occur during a period of 100 BUSCLK- cycles (40ms at 2.5MHz) then the transmission of the interrupt code is repeated and the 'LS490 triggers the left flip-flop again.

A further example of arbitration logic is shown in section 7.3.

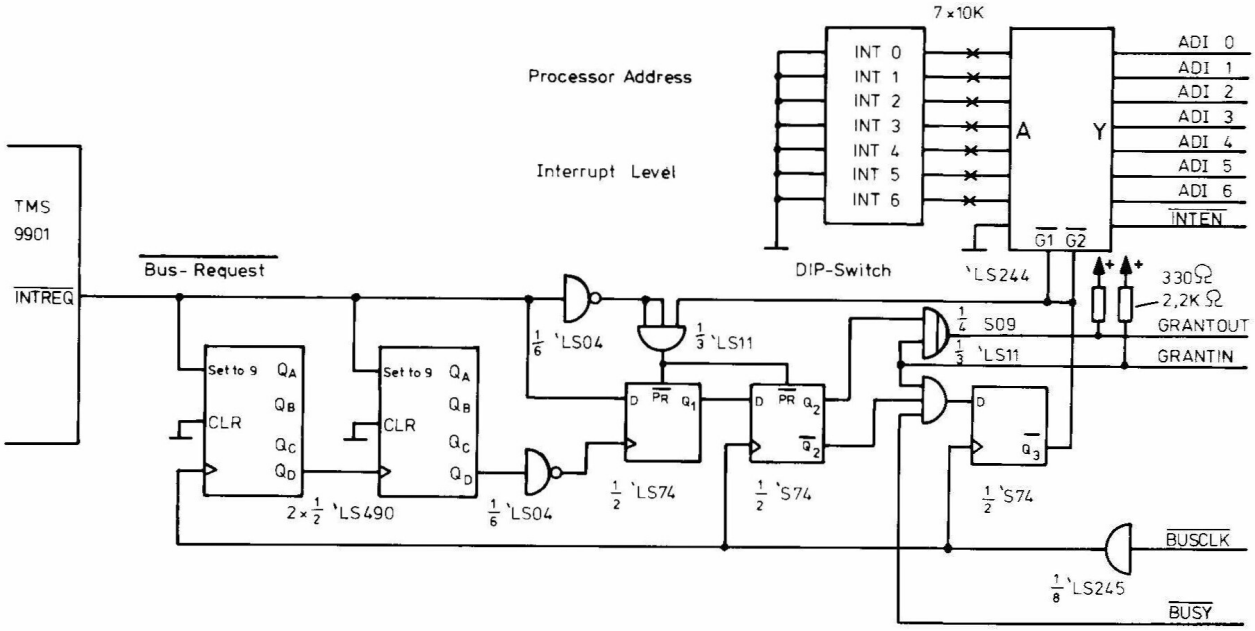


Figure 6-3 Bus Arbitration Logic of the TM990/E350 Module

6.4.2 CALCULATION OF SIGNAL PROPAGATION DELAYS

The timing constraints for an interrupt module bus arbitration can be construed from fig.6-4 and table 6-2. The times given form the basis for the design of the circuit

shown in fig.6-3. The following (worst case) calculation shows that the circuit is suitable for use with system frequencies of 2.5 and 4MHz. The various maximum propagation delay figures are taken from the TTL data book.

BUSCLK- to INTEN- (LOW)			BUSCLK- to GRANTOUT (HIGH)		
´LS245	tPLH	12ns	´LS245	tPLH	12ns
´S74	tPHL	9ns	´S74	tPHL	9ns
´LS244	tPZL	30ns	´LS11	tPHL	20ns
		----	´S74	tPLH	6ns
	tp =	51ns	´S09	tPLH	10ns
					----
				tp =	57ns

Two examples of a worst case calculation

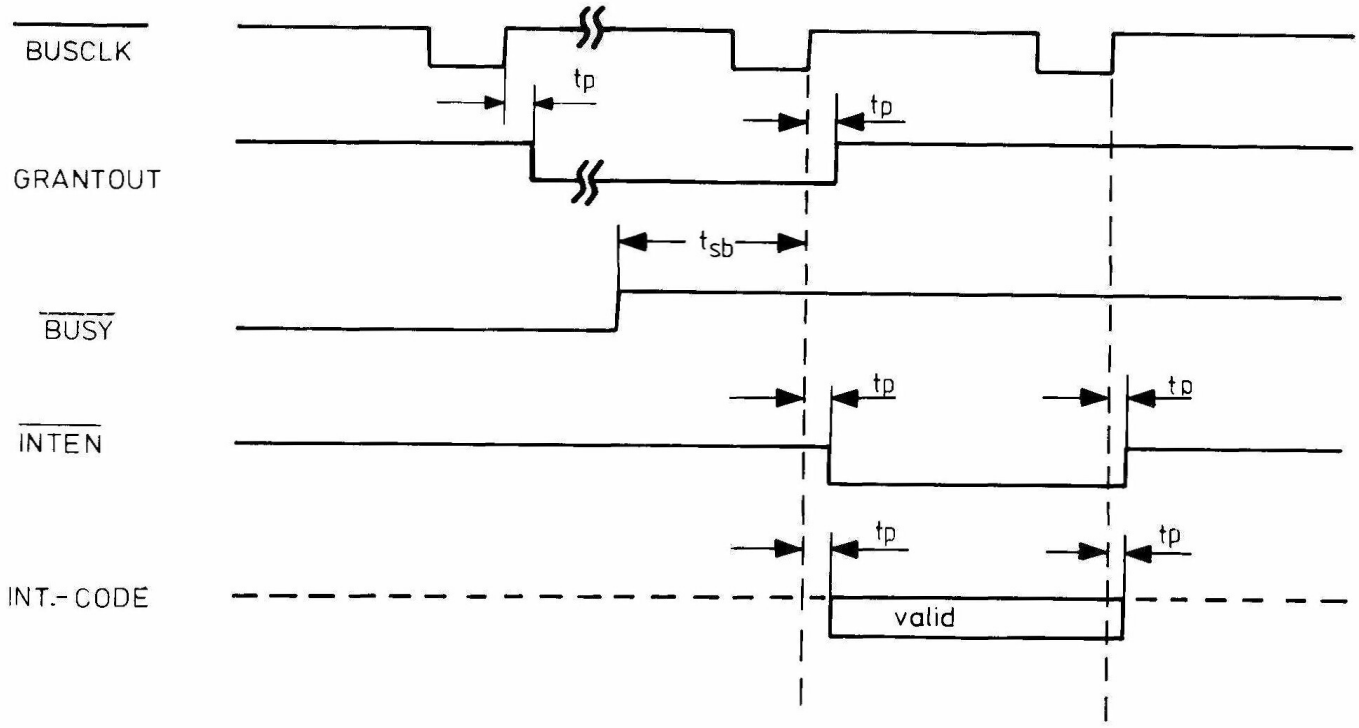


Figure 6-4 Bus Arbitration Timing Constraints

Table 6-2 shows that the maximum propagation delay (tp) should be 60ns (BUSCLK- up to 4MHz) and is thus achieved. The set-up time requirement of the BUSY- signal (tsb) is also fulfilled by the circuit shown in fig.6-3 since the difference between the delay times of the ´LS11 gate and the ´LS245 buffer is only 3ns.

Busclock frequency	Set up time	Delay time
2.5MHz	t1 > 30 ns	0 < t2 < 60 ns
4 MHz	t1 > 30 ns	0 < t2 < 60 ns
6 MHz	t1 > 20 ns	0 < t2 < 20 ns

Table 6-2 Bus Arbitration Timing Constraints

6.5 PROCESSOR MODULE INTERRUPT LOGIC

6.5.1 STATIC INTERRUPT SIGNALS

The three static interrupt signals PRES-, NMI- and PWRFAIL- are active LOW and remain on the E-BUS until the relevant interrupt source is reset. It is therefore not necessary to store these signals. A decoder (e.g. PROM) encodes the signals into the correct interrupt code for the microprocessor being used (see also table 6-3).

6.5.2 EVALUATION OF THE INTERRUPT CODE

The functional circuit diagram (fig.6-5) shows an example of the demultiplexing of the ADI bus signals. A microprocessor such as, for example, the TMS9981, requires a code to be present at its interrupt inputs (IC0 to IC2) for a minimum of two clock cycles to guarantee correct recognition. Since the TMS9981 also only interrogates its interrupt inputs at the end of an IAQ cycle this requires the interrupt code to be present for at least the duration of a complete IAQ cycle.

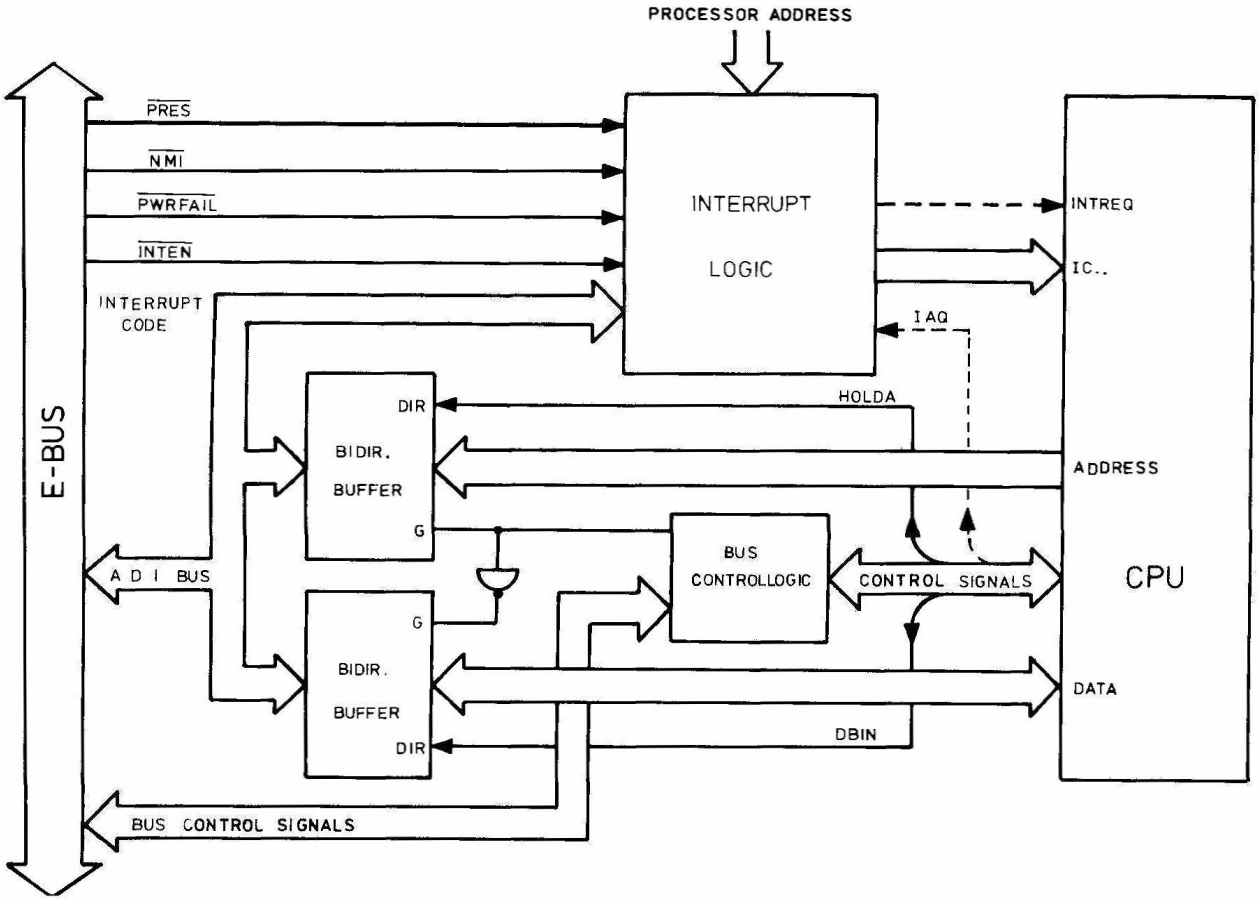


Figure 6-5 MC-Module Interrupt Operation

Fig.6-6 shows, simplified, the TM990/E150 processor module interrupt logic. The timing diagram shown in fig.6-7 indicates an indeterminate period between the transmission of the interrupt code and the beginning of the service routine (positive edge of the IAQ signal). This period results from the time required to complete the instruction currently being executed (see "Instruction Execution Times" table in the relevant microprocessor manual).

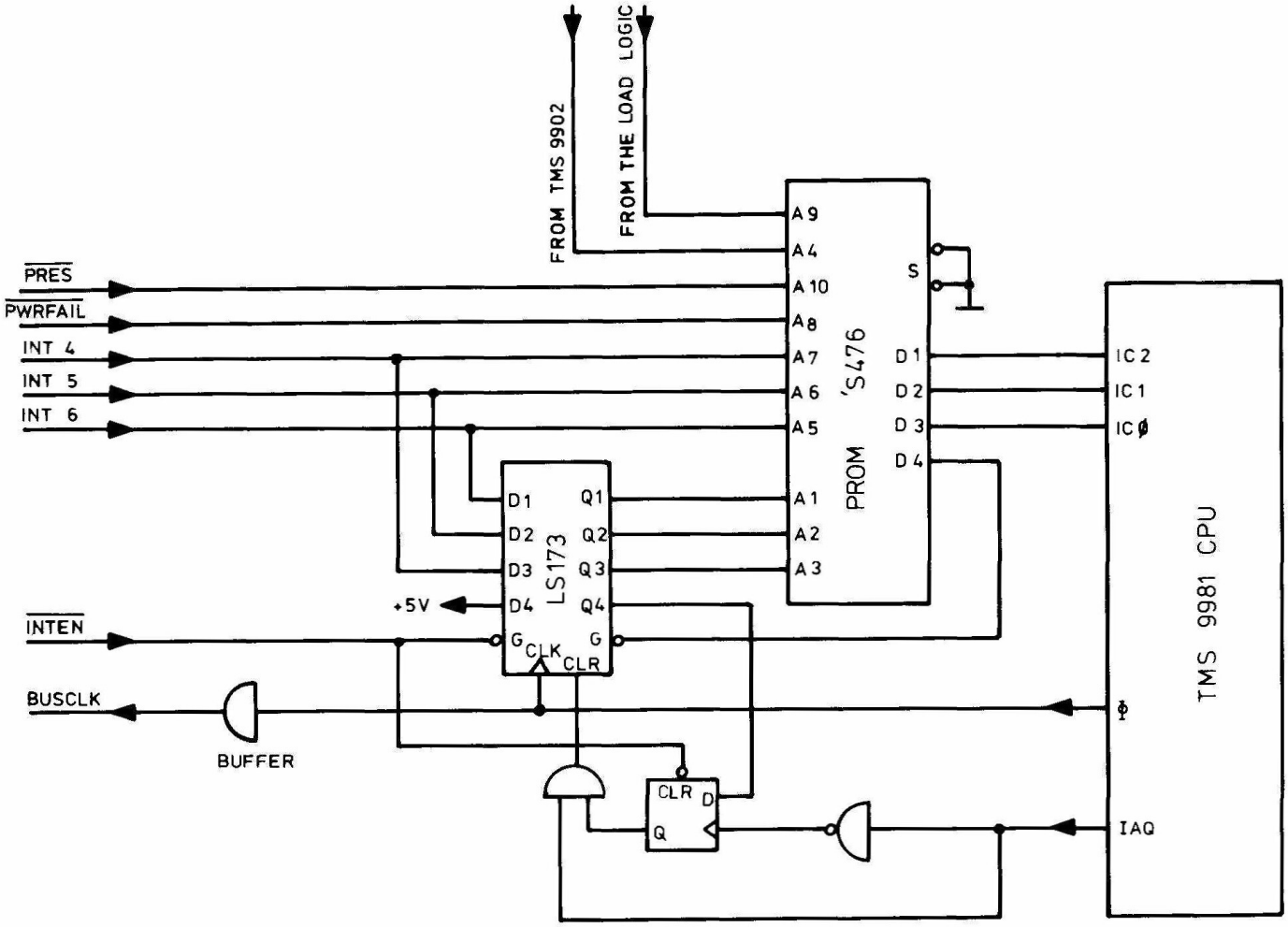


Figure 6-6 TM990/E150 Module Interrupt Logic

A processor module recognises the presence of an interrupt code on the bus by the INTEN- signal being active (LOW). Fig.6-7 shows that the interrupt code (INT4, INT5, INT6) is only latched into the 'LS173 4 bit register when both INTEN- and output D4 of the PROM are active LOW. This PROM output is LOW when the interrupt code transmitted (A5 to A7) has a higher priority than the code presently stored in the register (inputs A1, A2, A3). The static interrupt signals (inputs A4, A8, A9, A10) have a higher priority and are therefore fed immediately to the microprocessor inputs.

As shown in fig.6-7 the interrupt code is stored until the beginning of the next but one IAQ cycle. At this time the TMS9981 is executing the first command of the interrupt service routine so the code need no longer be stored. This guarantees complete software transparency of the processor module interrupt logic (reset of the interrupt latches follows automatically), and after the 'LS173 has been reset, a lower level interrupt code can be accepted.

Table 6-3 shows the programming of the ´S476 PROM shown in fig.6-6. It should be noted that the E-BUS interrupt code is not identical to the interrupt code of the TMS9981. The interrupt sources PWRFAIL- and level 1 share interrupt vectors, as do level 4 and the TMS9902 serial interface circuit interrupt. If, in a program, both level 3 interrupts can be active it is possible to distinguish between them by using CRU bits >140 to >17E (R12) (see also table 5-3). A bit from this CRU range is read as LOW if the E-BUS PWRFAIL- line is active.

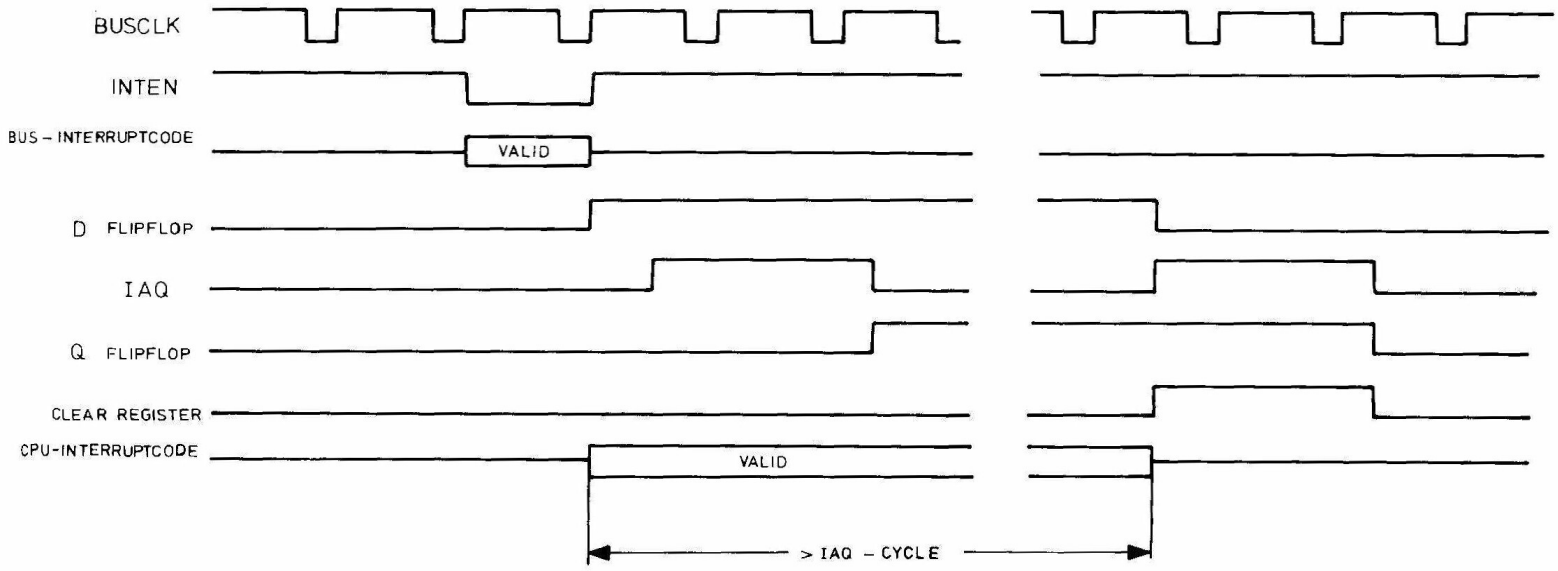


Figure 6-7 Timing Diagram for Fig.6-6

Interrupt level	Interrupt source	E-BUS interrupt code I0	I1	I2	I3	I4	I5	I6	TMS9981 IC0	IC1	IC2	TMS9981 function
1	PRES-	static interrupt							0	0	0	RESET
2	NMI-	static interrupt							0	1	0	LOAD
3	PWRFAIL-	static interrupt							0	1	1	Level 1
3	Level 1	x	x	x	x	0	0	1	0	1	1	Level 1
4	Level 2	x	x	x	x	0	1	0	1	0	0	Level 2
5	Level 3	x	x	x	x	0	1	1	1	0	1	Level 3
6	Level 4	x	x	x	x	1	0	0	1	1	0	Level 4

x=optional

Table 6-3 TM990/E150 Module Interrupt Levels

The TM990/E150 module is a single processor module with 6 interrupt levels and therefore ignores bits 0 to 3 of the interrupt code. The evaluation of the processor address, as

indicated in fig.6-5 (bits 0 to 2 of the code), is only required in multi-processor systems. On a multi-processor module the addresses may be set up using DIL switches and then loaded into the interrupt logic by an initialisation routine.

6.6 SERVICE ROUTINE PROGRAMMING

When programming an interrupt service routine, care should be taken that the interrupt source is reset as quickly as possible. In practice this has the following advantages:

1. Minimise unnecessary E-BUS contention (for example by a module re-transmitting the interrupt code every 100 BUSCLK- cycles*). Modules having lower priority are therefore not interrupted unnecessarily (e.g. access of a processor module to an external register).

   * 100 bus clock cycles corresponds to the execution of about five commands on a TMS9981

2. During the return from an interrupt service routine using the RTWP command, the microprocessor status register is restored, re-enabling interrupts at the level just serviced. If the command to reset the interrupt source is at the end of the service routine immediately before the RTWP, it can happen that an interrupt is sent just after fetching - but before executing the reset instruction. this interrupt code will be latched on the CPU board and recognized after execution of the RTWP instruction - as a new interrupt ! (for which the source has already been reset !) This can cause errors in program execution which are, as a rule, very difficult to trace.

WARNING

The module interrupt source must be reset at the latest two instructions prior to the return into the main program. Failure to do so can result in the service routine being accessed a second time since the E-BUS interrupt code, stored on the processor module, can require two instruction execution times before it is cleared.

6.7 INTERRUPT PRIORITIES

In discussing the priority of an interrupt it is necessary to differentiate between the priority of an interrupt level and that of a slot position.

6.7.1 INTERRUPT LEVEL PRIORITY

The priority of an interrupt level is determined using bits 3 to 6 of the transmitted interrupt code. This code determines, via the associated interrupt vectors, which service routine is to be executed.

The interrupt mask (in the microprocessor status register) determines the level of the lowest free interrupt and must be loaded initially using the LIMI command (load interrupt mask). During the execution of a service routine the mask is automatically set to the value of the next highest interrupt level hence a service routine may only be interrupted by a higher priority level interrupt (see also table 6-3).

6.7.2 SLOT PRIORITY

On a standard E-BUS backplane (e.g. TM990/E5012), the slot position determines the bus arbitration priority of that module. A slot at the beginning of the daisy chain (GRANT) line has the highest priority. Example: if the modules of the system are so arranged such that the component sides (as seen from the front) are to the right, then the left most slot has the highest priority. The GRANTIN input on a module in this slot is HIGH and its GRANTOUT output controls all lower priority modules.

The possibilities of parallel priority control are explained in section 3.2.2.

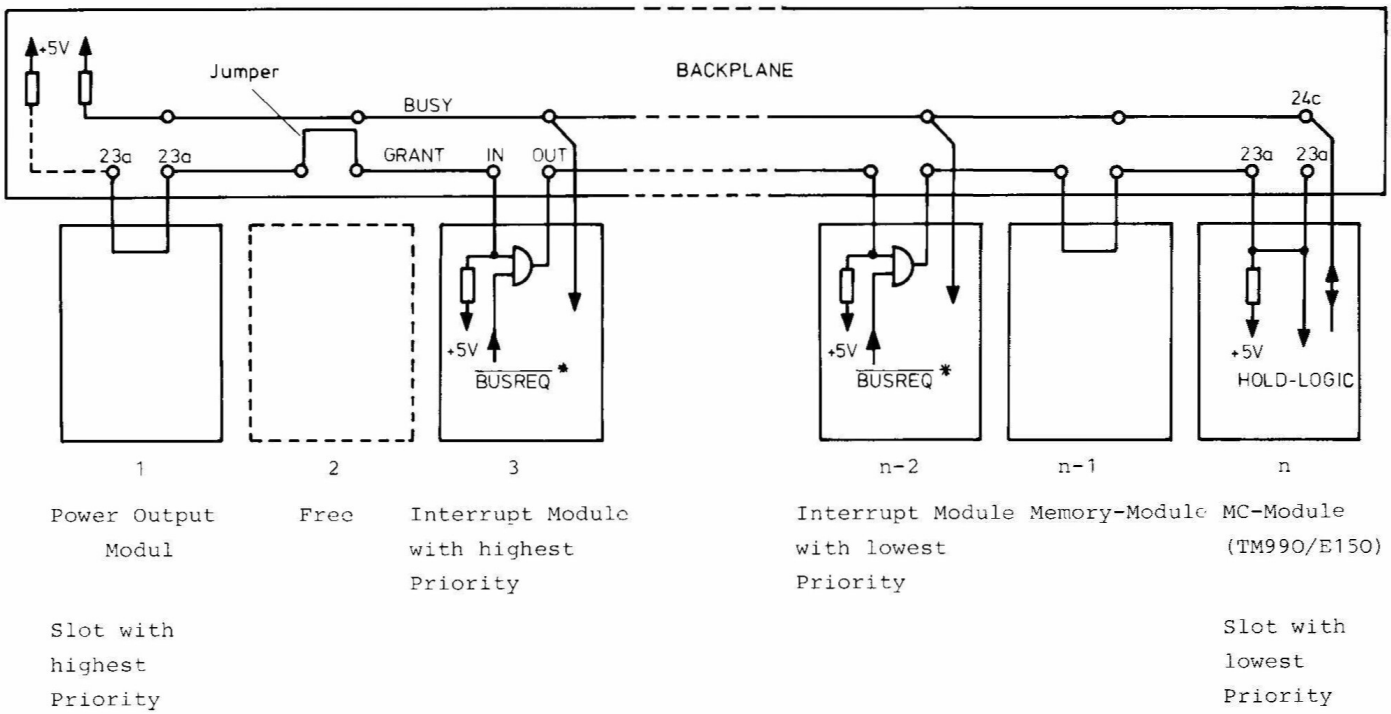


Figure 6-8 Arrangement of Different Modules

6.7.3 SLOT SELECTION

For safe interrupt operation, the physical location (slot) of an interrupt module (a module that transmits an interrupt code) should be such as to give it a higher priority than a receptive processor module. This can be explained with reference to the TM990/E150 (single master) MC- or MMC-module:

The TM990/E150 MC-module microprocessor is forced into the HOLD mode via the GRANT input, switching all bus drivers into the input or 3-state conditions. The module signifies this mode by setting BUSY- HIGH and only generating BUSCLK-, which is required for the synchronisation of all bus arbitrations.

If a processor module is in a slot having a higher priority (i.e. to the left of an interrupt module) then the interrupt module cannot control the GRANT input (see also fig.6-8). Thus the MC-module does not free the BUSY- line and hence the interrupt module cannot access the bus.

From the example shown in fig.6-8 it can be seen that the GRANT line between an interrupt and a MC-module must not be arbitrarily broken. On modules without bus arbiters the

GRANTOUT signal can be linked directly to GRANTIN on the board while on free slot positions the two signals may be linked directly on the back plane.

6.8 INTEN- AS A COMMON INTERRUPT REQUEST LINE

In small E-Systems, CRU expansion chassis or with MC-modules having only one bus interrupt the INTEN- line can be used as a common interrupt request line. This can be accomplished by using an open collector driver connected directly to the interrupt source. The bus arbitration logic (if present), should be disabled in this mode, e.g. by a jumper. Fig.6-9 shows the extended arbiter logic of the IN-module TM990/E350 which is capable of operating in either mode.

Interrupt service routines must poll all modules connected to the INTEN- line to identify the interrupt source.

The OEM-MC-modules TM990/E151 and TM990/E155 both use the INTEN- line as a common static interrupt request line.

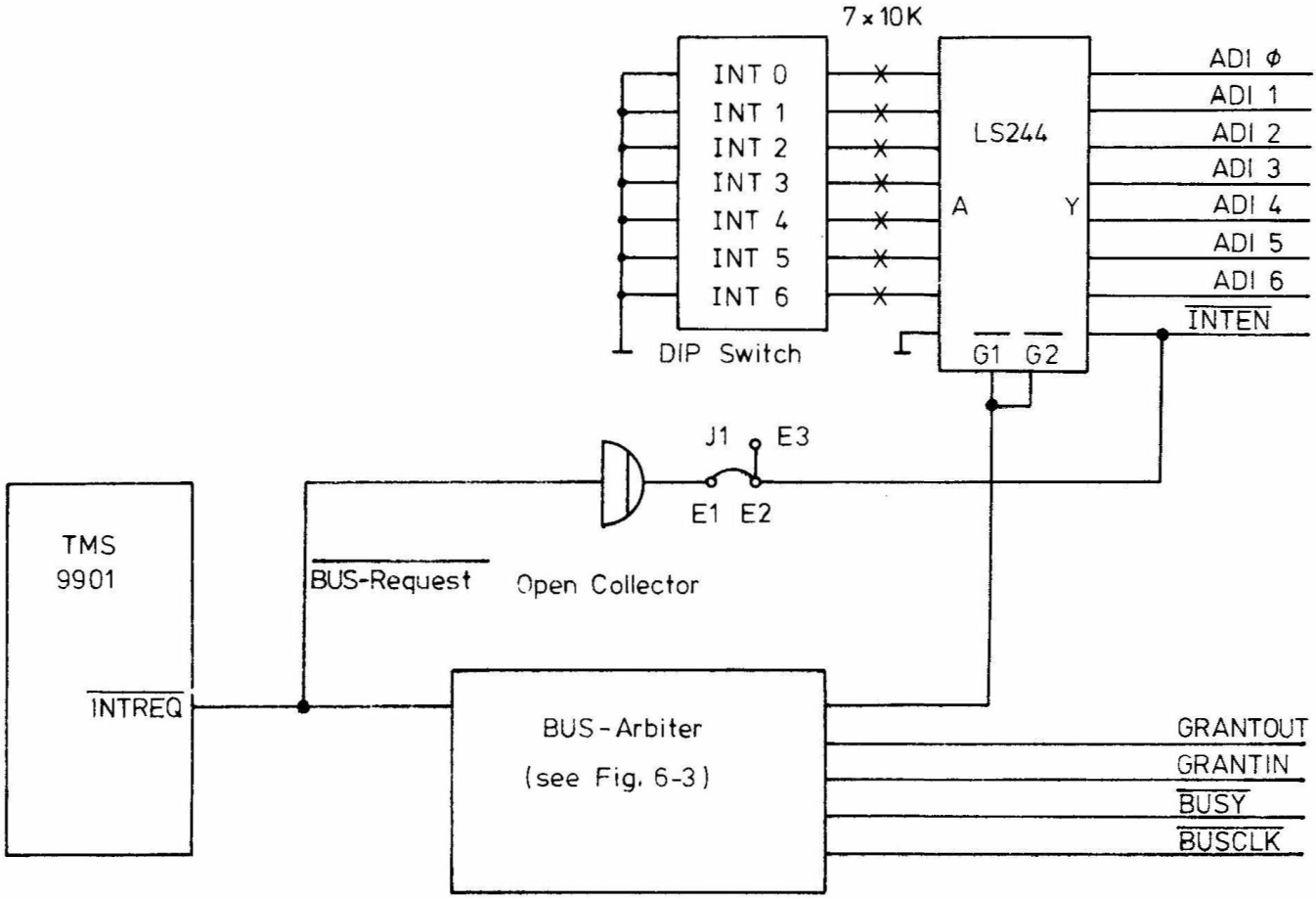


Figure 6-9 Static Control of INTEN-

6.9 BUS ARBITRATION CONTROL SIGNALS

The following list summarizes the E-BUS control signals which must be monitored or controlled by an interrupt module.

BUSCLK- All bus arbitrations are synchronised at the positive edge of BUSCLK- (active LOW).

BUSY- BUS BUSY- (active LOW) shows that a module is accessing the bus.

INTEN- INTEN- (active LOW) shows the presence of an interrupt code on the multiplexed ADI bus.

IORST- IORST- (active LOW) forces all E-BUS interrupts to be reset.

GRANTIN GRANTIN being LOW indicates that a higher priority module is requesting the bus.

GRANTOUT A module sets GRANTOUT LOW to indicate that it is requesting bus arbitration.

SECTION 7

CIRCUIT EXAMPLES

7.1 PARALLEL 16 BIT I/O INTERFACE

The circuit shown in fig.7-1 shows the use of the TMS9901 programmable system interface circuit with the E-BUS CRU interface. The TMS9901 provides up to 16 ports, programmable as inputs or outputs, as well as providing up to 16 static (active LOW) interrupt inputs. The input/ output ports are set into a high impedance state when a reset is invoked (soft or hardware reset). The TMS9901 has a programmable timer, with a resolution of 25.6us (with a BUSCLK- frequency of 2.5MHz) and a maximum time interval of 419.4ms, and uses interrupt level 3. A 7 pole DIL switch enables the CRU base address to be relocated anywhere within the CRU address space in 32 bit steps.

The circuit example shown in fig.7-1, like the TM990/E352 module (universal I/O), uses the TMS9901 interface circuit. However, the interrupt operation differs considerably. The TMS9901 interrupt code (IC0 to IC3) is fed directly to the E-BUS via the ´LS374 latch and occupies all the processor module interrupt levels. The TM990/E352 module on the other hand has only one interrupt level, selectable with a DIL switch.

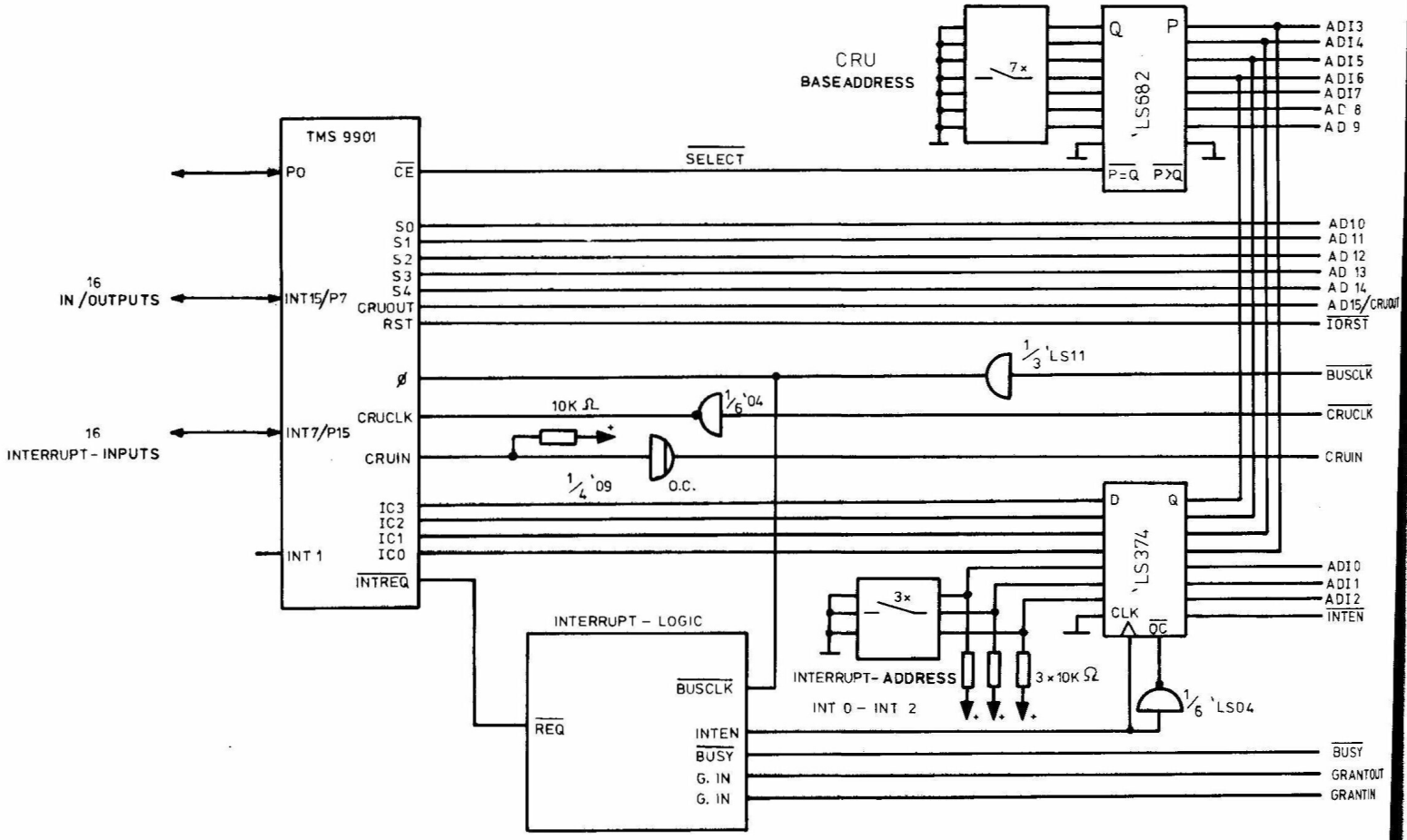


Figure 7-1 16 Bit Parallel System Interface

The TM990/E150 processor module only allows six levels of interrupt and therefore bit INT3 of the interrupt code is ignored (see also table 5-3). This has the effect of only utilising interrupt inputs INT1 to INT4 of the TMS9901 while interrupt inputs INT9 to INT12 are wired-or with interrupt inputs INT1 to INT4, i.e. they use the same interrupt vectors.

7.2 SERIAL TERMINAL INTERFACE

The following example shows the production of an EIA RS-232C or TTY interface using a TMS9902 or TMS9903 in conjunction with the E-BUS CRU interface. The TMS9902 is an asynchronous interface circuit while the TMS9903 produces a synchronous interface. The ICs are pin compatible, although the TMS9903 has two additional pins in comparison with the TMS9902.

In this example, combinational logic is used to produce a CRU base address for the TMS9902/3 of >0180 (R12) resulting in a CRU address range of >180 to >19E for the TMS9902/3. The evaluation of the MEMEN- line, as indicated, is not strictly required, as the TMS9902/3 only assumes valid data on the CRUOUT line with the active state of CRUCLK-.

The four TMS9902/3 interrupts are connected internally to a common output (INT) which thus uses a common interrupt level - which may be set, for example, by a DIL switch. A circuit example for the interrupt logic as indicated (bus arbiter) is described in section 6.4 of this handbook.

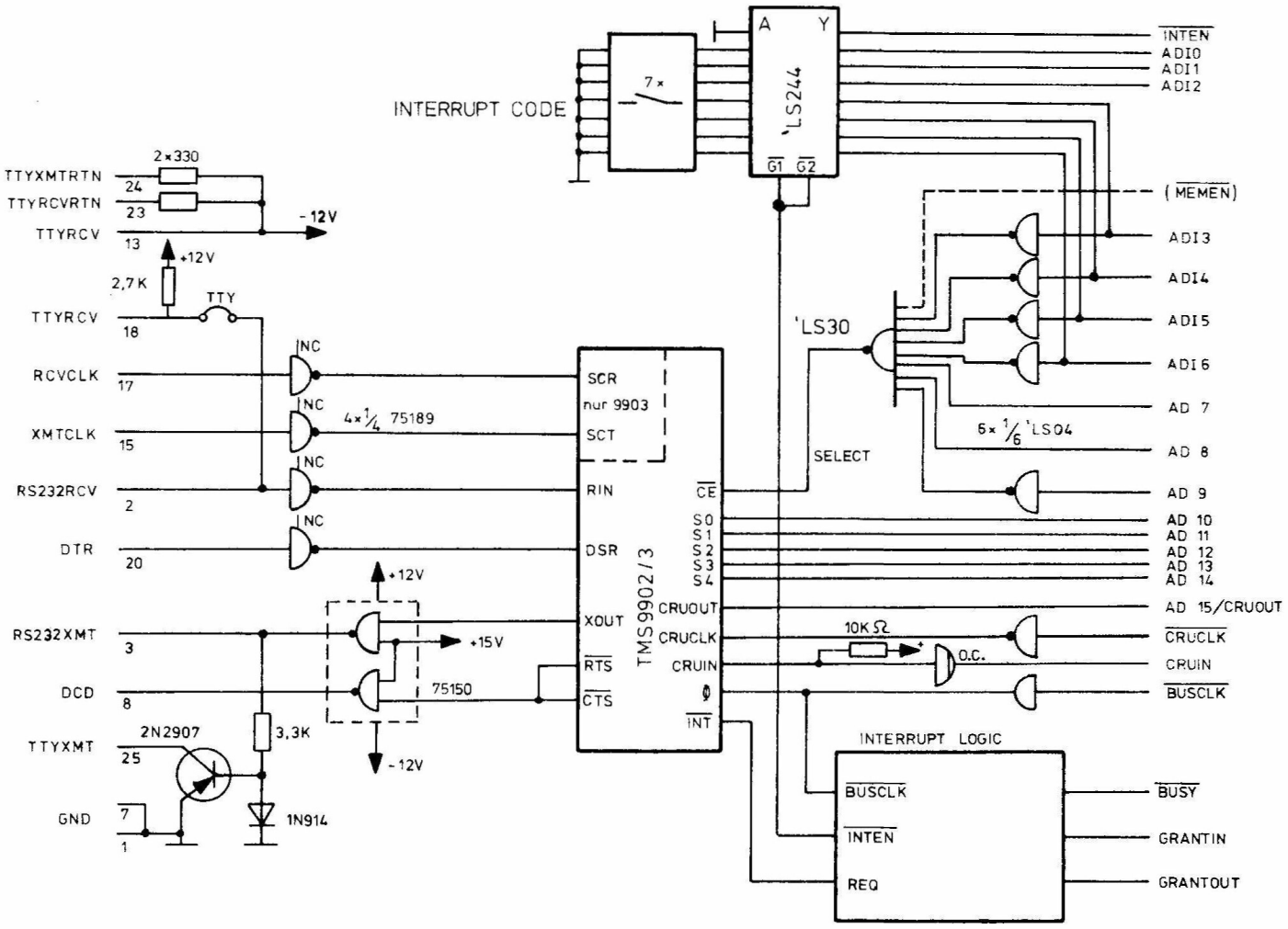


Figure 7-2 Serial Terminal Interface

The TM990/301 microterminal may be used instead of a terminal or printer, however additional supply lines (+5V and +12V) must be added to the connector pins (see table 9-4).

7.3 EDGE TRIGGERED INTERRUPT INTERFACE

The following circuit gives a further example for logic suitable for the transmission of the interrupt code (bus arbiter). It differs from that shown in fig.6-3 by the following:

1. The timing for the repetitive transmission of the interrupt code is produced using a monostable and is therefore independent of BUSCLK-.

2. The interrupt code is not produced by a DIL switch but is loaded into a register by the initialising microprocessor.

7.3.1 FUNCTIONAL DESCRIPTION

The method of interrupt code programming shown here facilitates the production of an interrupt module having multiprocessor capability, i.e. initialisation can be achieved by other than a specific processor module. This is possible since the interrupt address is not determined by the hardware. The lowest value bit of the interrupt code (INT6) differentiates between the two interrupt inputs (INT.A and INT.B). Both interrupts then have related interrupt levels with INT.A having the higher priority.

The E-BUS line IORST- provides an indirect reset of the whole circuit thereby disabling both interrupt inputs. In this example the E-BUS CRU interface is used to initialise the circuit (i.e. enables one or both of the interrupt inputs). The following table shows a suitable address map.

relative CRU bit	function
0	interrupt code INT0, processor address (MSB)
1	interrupt code INT1, processor address
2	interrupt code INT2, processor address (LSB)
3	interrupt code INT3, interrupt level (MSB)
4	interrupt code INT4, interrupt level
5	interrupt code INT5, interrupt level
6	enable INT.A (HIGH), reset/disable INT.A (LOW)
7	enable INT.B (HIGH), reset/disable INT.B (LOW)

Table 7-1 Interrupt Interface CRU Address Map

During initialisation, the interrupt code is written into bits 0 to 5 using the LDCR command, and a "1" is written into bit(s) 6 and/or 7. A positive edge occurring at one of the

inputs triggers the corresponding flip-flop and enables, via the ´LS00 and the ´S08, the logic to request bus arbitration. The positive edge of the "Int.-Request" signal (see fig. 7-3) simultaneously triggers both monostables. On the next positive edge of BUSCLK-, the left ´S113 flip-flop drives the GRANTOUT output LOW and requests arbitration of the bus. After arbitration, the ´LS374 octal latch feeds the interrupt code and the INTEN- signals to the bus.

The resetting of an interrupt is achieved by writing a "0" to the relevant CRU bit. The monostable RC network determines the delay until the repetition of the bus arbitration, and is therefore programmable over a wide range. As long as the CLEAR input of the left ´LS123 is HIGH, the device operates as an astable multivibrator and every negative edge at its Q output re-triggers the succeeding flip-flop (an ´LS132 which is configured as an RS flip-flop by connecting the RC terminals to GND). During transmission of the interrupt code the flip-flops are reset.

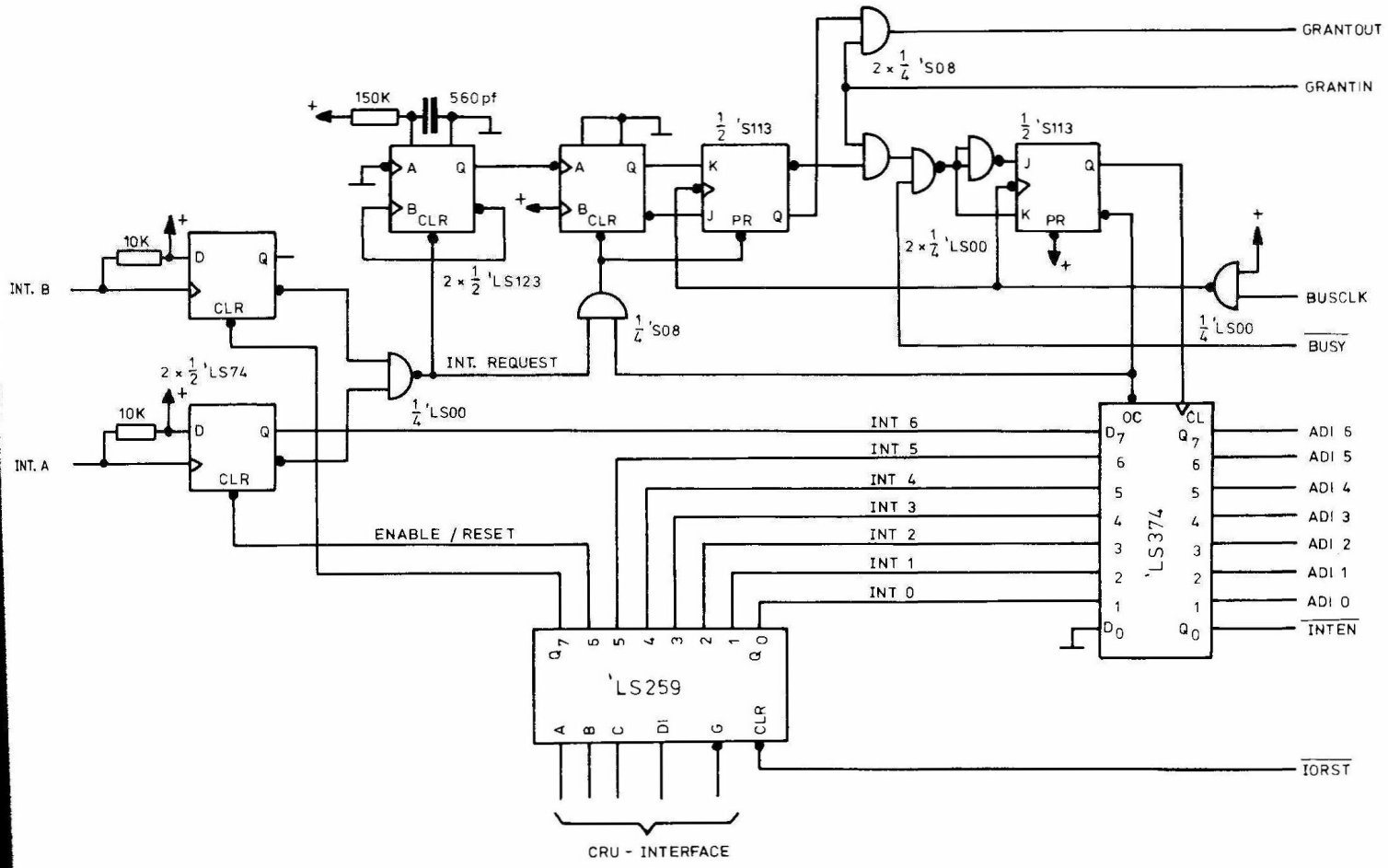
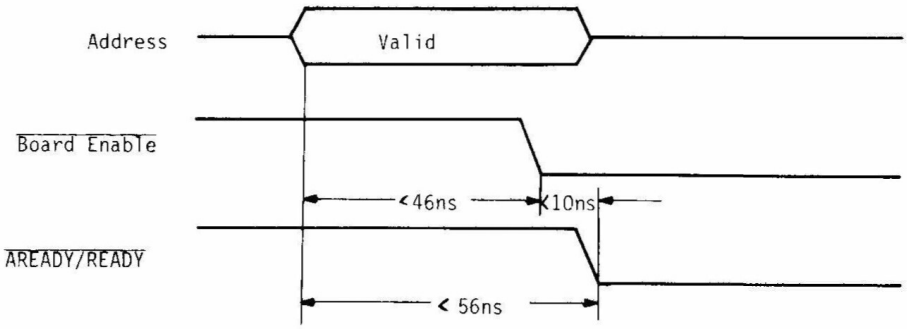


Figure 7-3 Edge Triggered Interrupt Interface

7.4 UNIVERSAL MEMORY MAPPED INPUT/OUTPUT

The following circuit diagram shows a universal memory mapped input/output interface for E-BUS. This interface may be used with processor modules which utilise either an 8 bit or a 16 bit wide data bus. The circuit incorporates 32 of both input and output bits, and expansion, without substantial alteration in the address decoding, is relatively easy to achieve. The address decoding functions over the range 0 to >3FC0 having a step increment of >40. The 6 highest value address bits A1 to XA0 are decoded and must all be LOW.

The following timing diagram shows that the circuit illustrated in fig.7-4 fulfills the critical timing constraints placed on the address decoder relating to the READY- signal. The use of LS circuits having negligible delay times ensures that no WAIT-STATES are required.



READY-/AREADY- Logic Timing Diagram

This example circuit is capable of working with either 8 or 16 bit wide data depending on the value of MEMWIDTH. If dual-width operation is not required, then one or two (depending on the desired mode) bidirectional data drivers and the associated MEMWIDTH logic can be omitted.

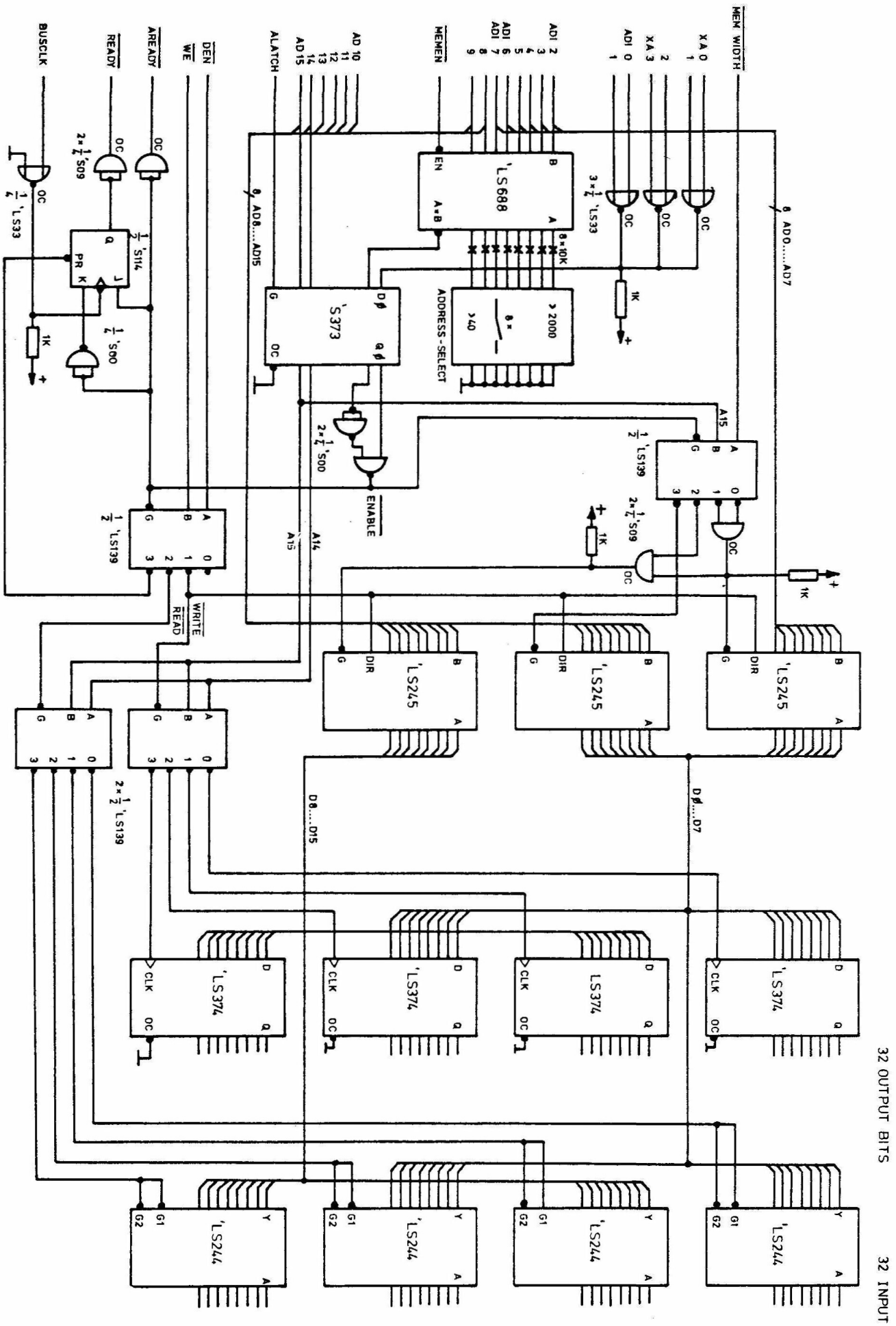


Figure 7-4 Universal Memory Mapped I/O Interface

7.5 ANALOGUE-DIGITAL CONVERTER INTERFACE

The ADC0816 analogue-digital converter shown in the following circuit example (fig.7-5) has an 8 bit resolution and 16 multiplexed analogue inputs. The address decoding used is identical to that shown in fig.7-4 and the MEMWIDTH signal need not be decoded since the ADC0816 has only an 8 bit wide output.

If, for example, the interface start address is mapped to >3000 using the DIL switch, then the analogue input IN10 may be accessed using the command "MOV R0,@>300A" which also initiates the conversion. The ADC0816 indicates the end of a conversion by a positive edge at the EOC output, which, via the ´LS74 flip-flop, produces an interrupt request. Figs 6-3 and 7-3 give examples for suitable interrupt logic (bus arbiter). The result of the conversion may then be read using the command "MOV @>3000,R0" (note that the conversion result is always read at >3000, independent of the address of the previously selected analogue input).

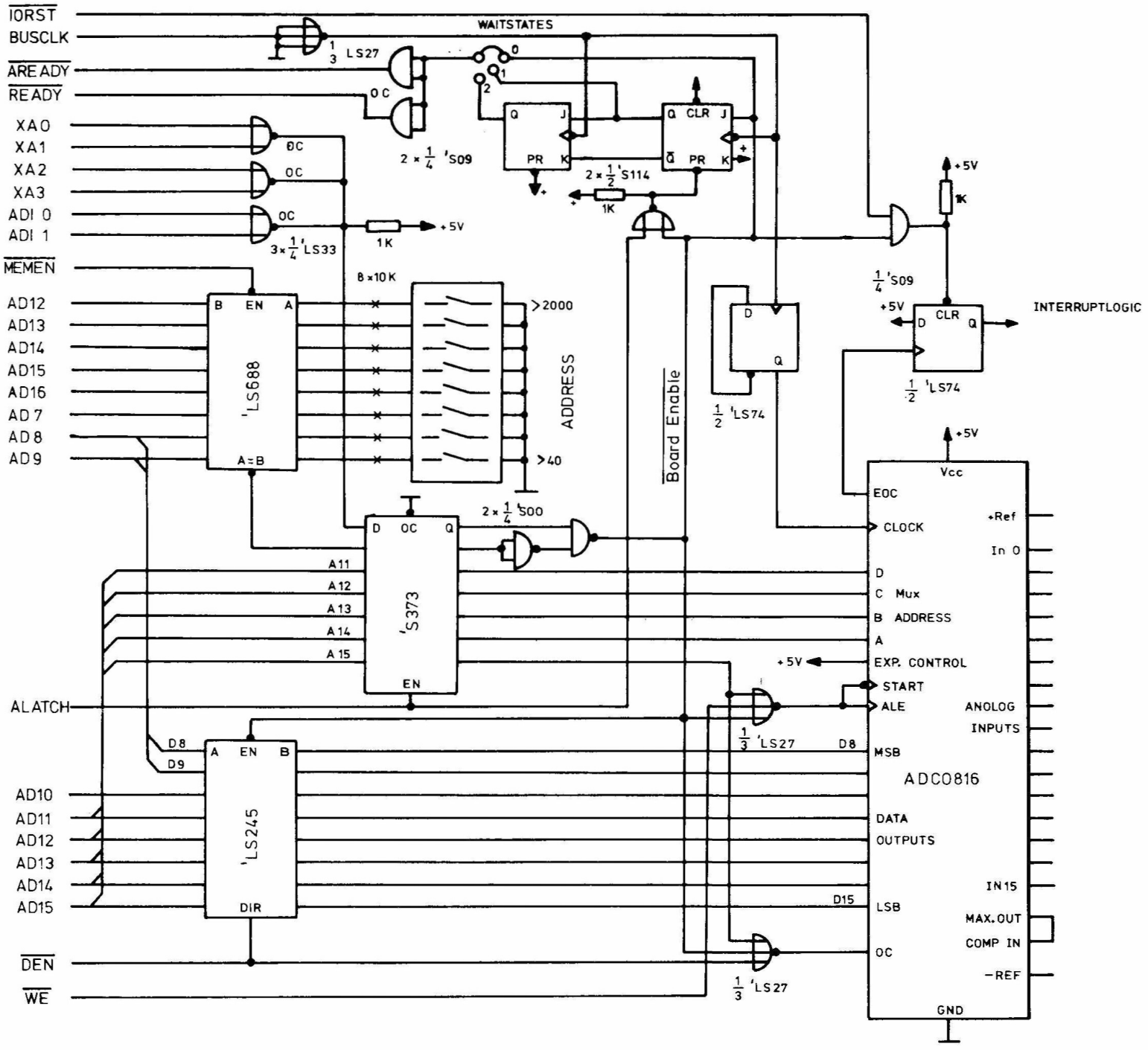


Figure 7-5 Analogue-Digital Converter Interface

7.6 E-BUS ARBITER

Fig.7-6 shows the discrete circuit of a bus arbiter for MMC-modules. By fulfilling the necessary conditions, this circuit controls the request, occupation and release of the bus. Asynchronously to other E-BUS modules, the logic requests a bus access as a result of an input on BRQ- and waits until the BEN- signal is active LOW. The BEN- signal signifies to all bus drivers that the E-BUS is available, thus enabling arbitration. The bus management signals GRANTIN, GRANTOUT and BUSY- are synchronous with BUSCLK-, and are defined in section 2.3.2.

If a module with higher priority requests the bus, then the DEN- and WE- signals indicate when the bus can be released, so that no data is lost. During the active LOW period of the LOCK input signal the E-BUS is locked to prevent access by any other module (see section 3.5.3).

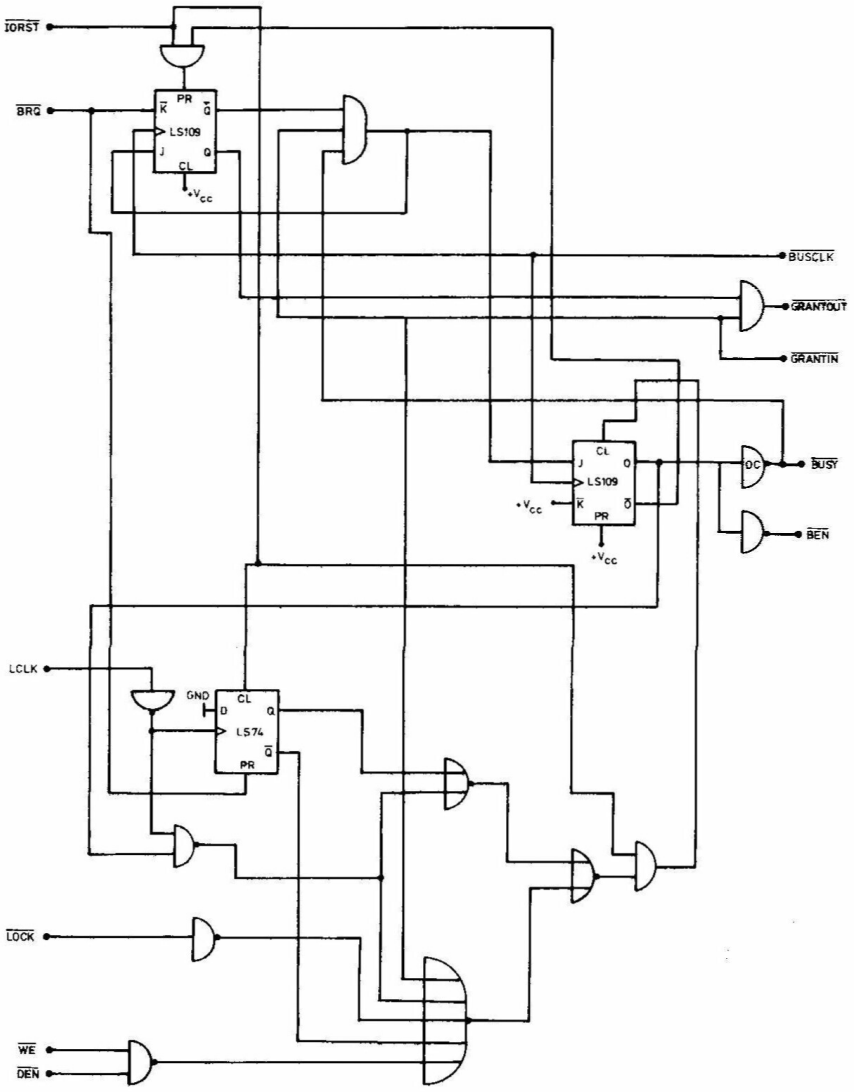


Figure 7-6 E-Bus Arbiter

SECTION 8

MECHANICAL ASSEMBLY OF E SYSTEMS

The following sections give the mechanical specifications of card formats, recommended connectors, chassis and mains supplies for E-systems.

8.1 CARD FORMAT

The most widely used card format in E-Systems is the 100mm x 160mm single Eurocard conforming to DIN 41494, part 2 (IEC 48D). Special applications such as input/output boards with back plane I/O connections, E-BUS couplers etc., can alternatively use the 233.44mm x 160mm double Eurocard format. Card dimensions with tolerance limits are shown in table 8-1.

Card dimensions (mm)	Single Eurocard		Double Eurocard	
	Nominal	Tolerance	Nominal	Tolerance
length	160	+/-3	160	+/-3
width	100	-0.3	233	-0.3
board thickness	1.58	+/-0.08	1.58	+/-0.08

Table 8-1 Eurocard Dimensions

Fig.8-1 shows the two card formats giving dimensions and also the location of the connectors.

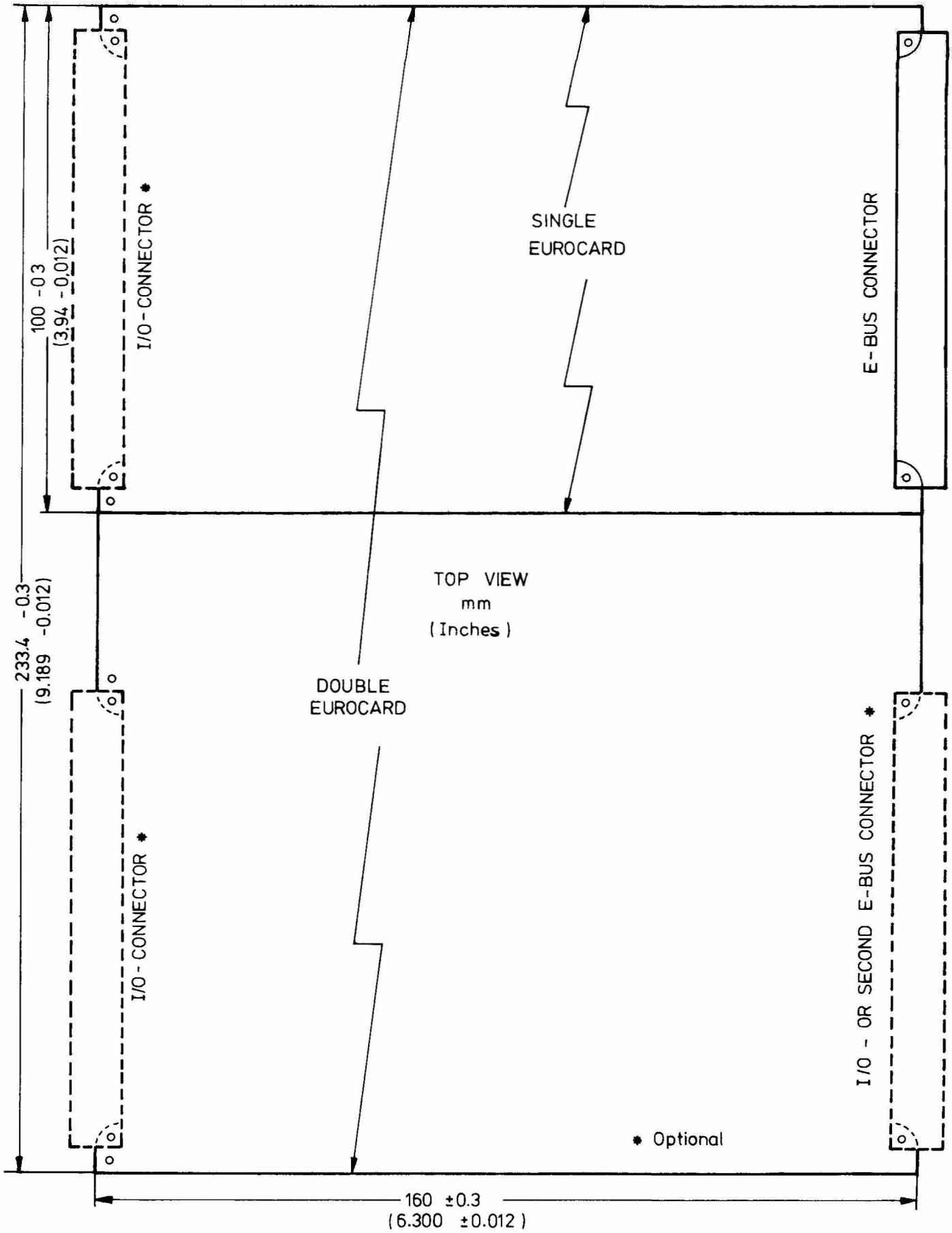


Figure 8-1 Card Formats and Connector Locations

8.1.1 SINGLE EUROCARD FORMAT

The single Eurocard, having a height of 100mm (3HE front panel height, HE = 44.31mm) and a length of 160mm can have one or two DIN 41612 connectors. The rear connector is dedicated to the E-BUS interface while the front connector may be used for input/output and/or display and servicing devices (e.g. LED displays, RESET switches etc.). Fig. 8-2 gives detailed dimensions of the single Eurocard format and includes hole locations for both front and back connectors (DIN 41612, 64 pin Type C). If the 64 pin, Type C, is not used for the DIN front connector then the hole locations may vary according to the version used (e.g. Type F etc.).

If a DIN front connector is not used, then it should be noted that the distance "Y" is changed to 3.57mm.

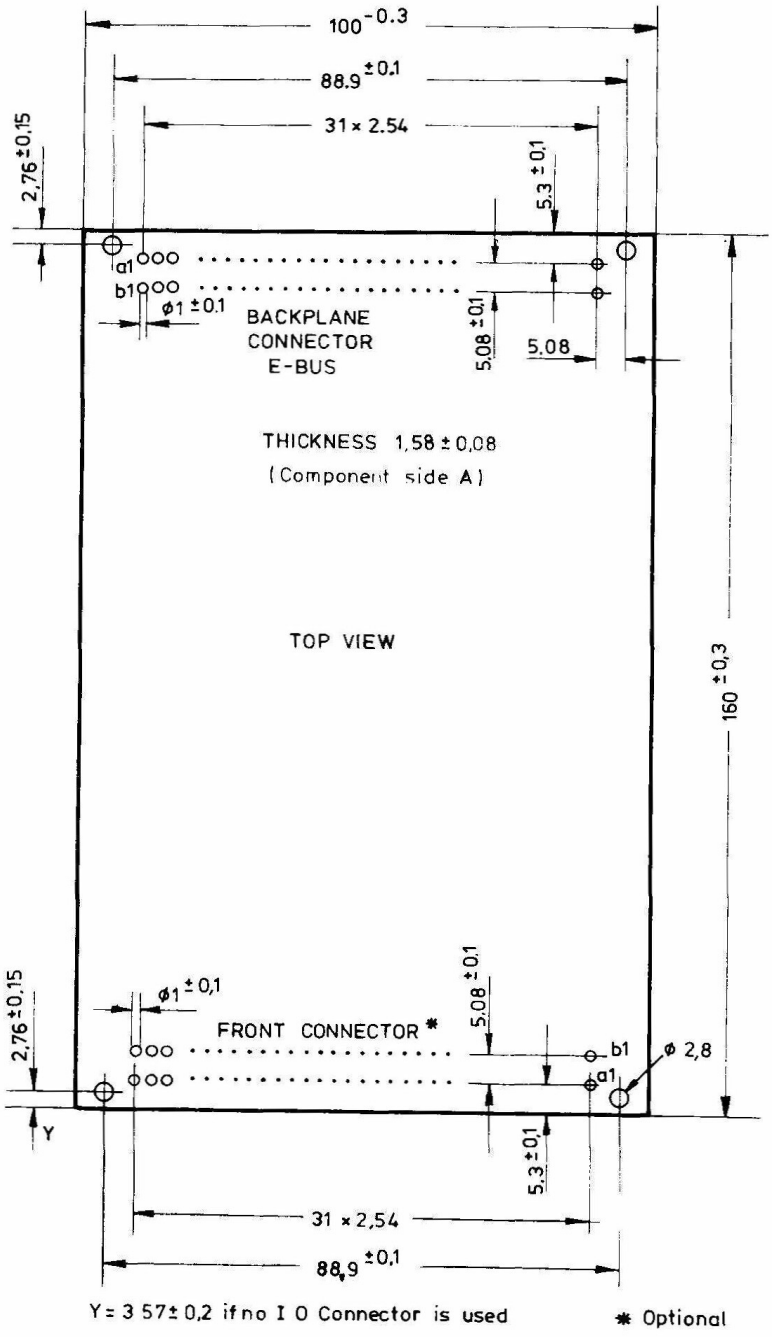


Figure 8-2 Single Eurocard Dimensions

8.1.2 DOUBLE EUROCARD FORMAT

The double Eurocard, having a height of 233.4mm (6HE front panel) and a length of 160mm, can have up to 4 DIN 41612 connectors. The upper back connector is assigned to E-BUS while the lower back connector may be used as a second E-BUS or input/output connection. The front connectors may be used as either input/output and/or servicing/display connections according to individual requirements. Fig.8-3 shows the dimensions and tolerances for the double Eurocard and gives possible connector locations. If a DIN front connector is not used, then the dimension "Y" becomes 3.57mm (see fig.8-3).

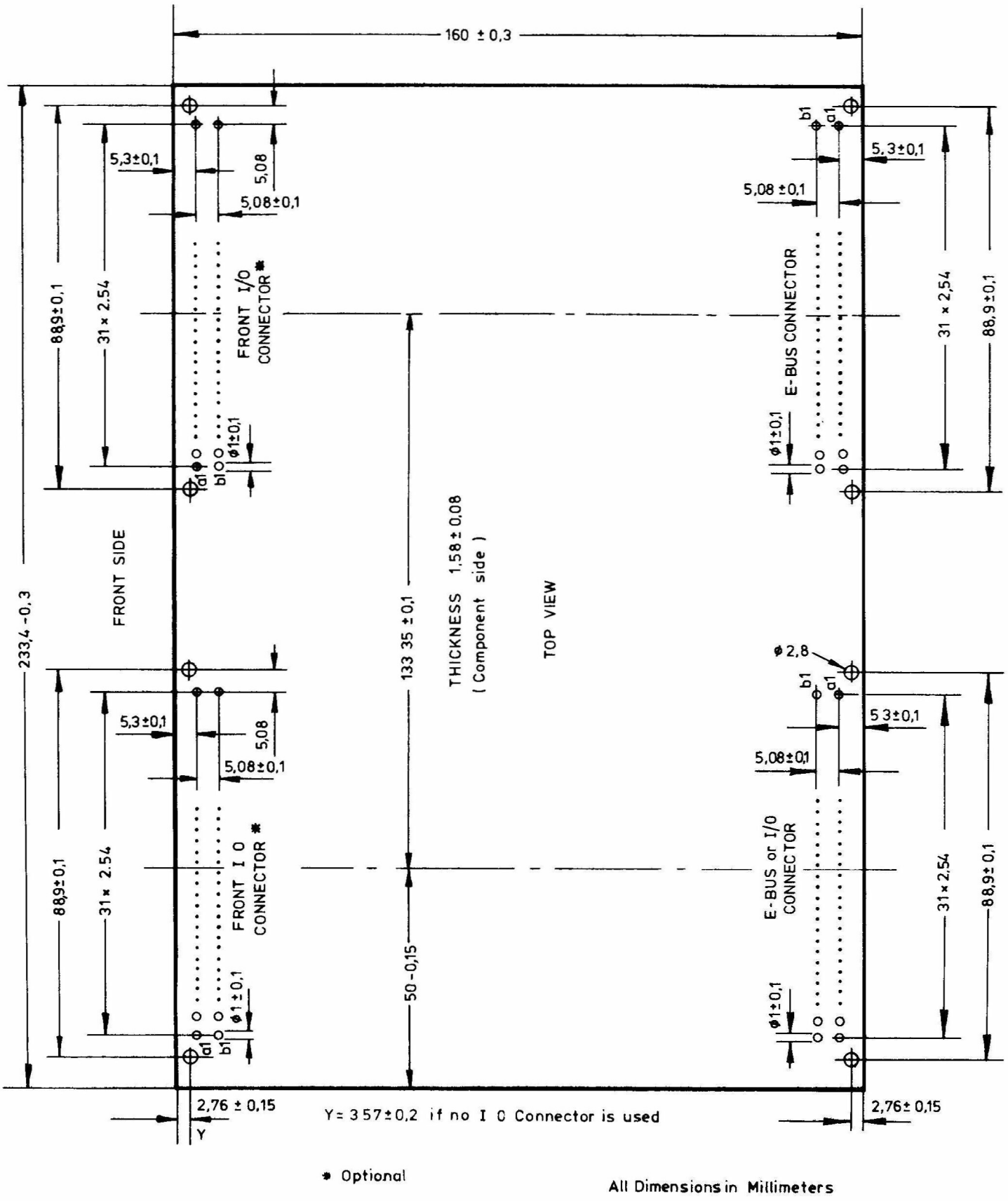


Figure 8-3 Double Eurocard Dimensions

8.1.3 CARD SPACING

Within an E-system, the distance between modules is 4TE = 20.32mm. Table 8-2 gives permissible dimensions relating to both the component and track sides of the board. The minimum gap between the components on one module and the under side of the next is 1.44mm.

	Min.	Nom.	Max.	Unit
Component side component height		10.00	15.00	mm
Board thickness		1.6		mm
Height on track side			2.88	mm
Gap between components and track side of next board (including screws etc.)	1.44	6.44		mm

Table 8-2 Board Spacing in E-Systems

8.2 CONNECTORS

In E-Systems the following types of connectors are possible;

- E-BUS connectors
- Input/output connectors
- Internal module connectors
- Mains connectors
- Peripheral equipment connectors

Connectors to DIN 41612 standards should be used for both E-BUS and input/output connections.

Internal module connectors should be selected to prevent interference with the front panel. Section 8.5 discusses the mains connection.

For peripheral equipment connections, it is necessary to distinguish between internal system connections (e.g. to a floppy disc) and equipment interface, such as to the EIA terminal etc.

8.2.1 E-BUS CONNECTOR

The connector used for E-BUS shall be the 64 pin DIN 41612 (part 2) type C (row B not used).

Male connectors are used on E-BUS modules (female connector on the back plane).

Male and female 64 pin DIN 41612, type C, connectors must conform to the specifications given in table 8-3.

	Min.	Typ.	Max.	
Contact resistance		15	20	mOhm
Current rating per contact (70 degrees C)	1.0	1.5		Amps
Insulation resistance	10E12			Ohm
Proof voltage	1000			V(eff)
Mechanical endurance	200	500		Cycles

Table 8-3 E-BUS Connector Specifications

The following DIN and IEC standards apply to E-BUS connectors:

	DIN	IEC
Construction overview	41612, part 1	130-14
Connector types B-D	41612, part 2	130-14
Test spec	41612, part 5 41630	130-1

8.2.2 DIN INPUT/OUTPUT CONNECTOR

Input/output connections to E-Systems in the industrial environment should utilise connectors to DIN standards. The following types are recommended.

	No. of Pins	Current/Pin Ta=70 deg.C	Signal Voltage
* C moulding (DIN 41612, part 2)	32-96	<1A	<48V
* F moulding (DIN 41612, part 3)	32-48	<4A	48-120V(eff)
* H moulding (DIN 41612, part 4)	15	<10A	<380V(eff)

Male connectors should be used on the board. Safety keying is provided as shown in fig.8-4 to prevent accidental reversal when the C moulding is used without a front panel.

The specifications and requirements of DIN 41612, part 5, and also the acceptance test DIN 41630 (IEC publication 130-14 and 130-1) should be adhered to. The type of connection to the pins on the input/output connectors (e.g. WIRE-WRAP, soldering, CRIMP, FAST-ON etc.) should be selected after consideration of these requirements.

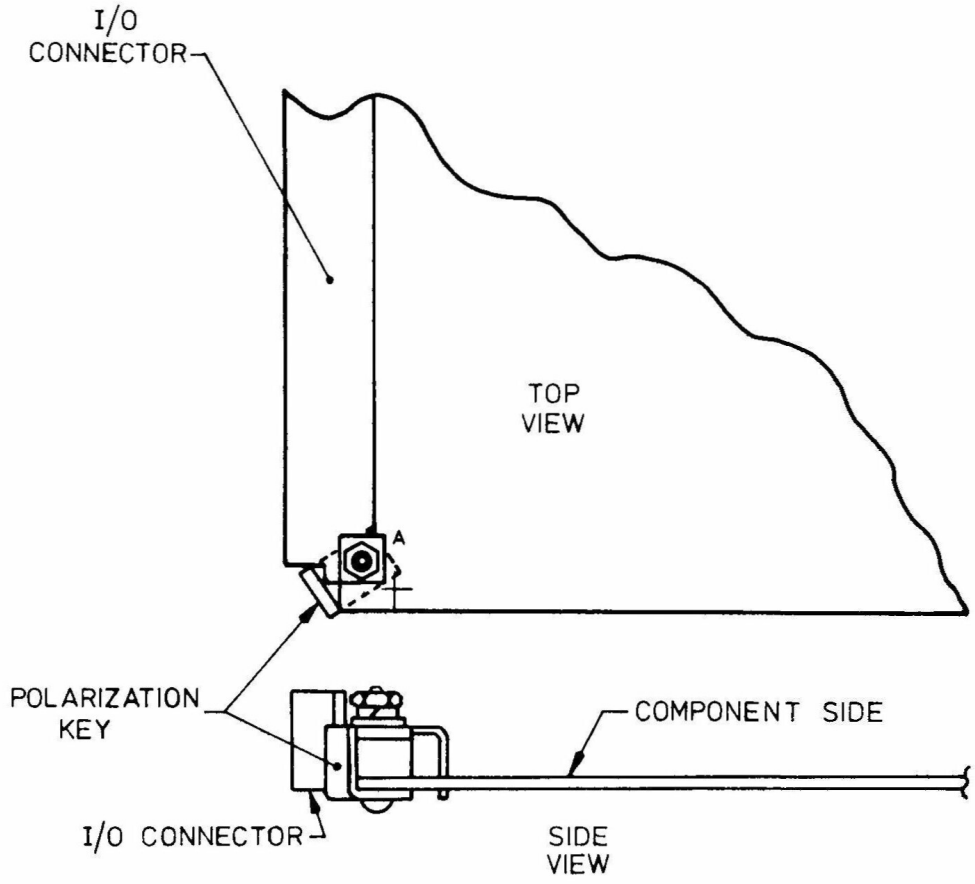


Figure 8-4 Input/Output Connector Type C - Polarization Key

8.2.3 PERIPHERAL CONNECTOR

For the case of a signal connection to peripheral equipment, it is necessary to differentiate between connections within a housing and those outside it. For signal connections to peripheral equipment within a housing or chassis, use of the 64 pin DIN 41612 type C male connector is recommended. Connection between a module and a peripheral control unit is then possible using ribbon cable (e.g. Scotchflex). For signal connections to peripheral equipment outside a housing or chassis, for example to an EIA terminal, printer etc., sub-miniature connectors should be used. E-Systems should adhere to the following international standards.

Standard Interface	No. of Pins/Type
-RS-232-C	25 pin/DP25
-RS-449	
* 2 channel (RS-422/423)	37 pin/DP37
* 1 channel (RS-423)	9 pin/DP9
-IEC 448	25 pin/DP25

The following pcb connectors are suitable.

No. of Pins	Type
9	HDP 207084-2+
25	HDP 206584-2+ or 206604-2*
37	HDP 206817-2+

\+ AMP or similar * for IEC bus connection

Fig.8-5 shows the location of the 25 pin connector. If the use of two 25 pin or several 9 pin equipment connectors is envisaged on the double Eurocard format, then locations should be selected that avoid interference with the front panel.

The E-System pin out for the serial RS-232C and TTY interfaces is shown in table 8-4. It should be noted that there are some changes from the standard arrangement (additional voltage supply, multidrop and 20mA line current connection).

The electrical specification of the symmetrical signal transmission is given in EIA-RS-422 (EIA = Electronic Industries Association). The RS-423 specification covers the transmission of an asymmetrical signal.

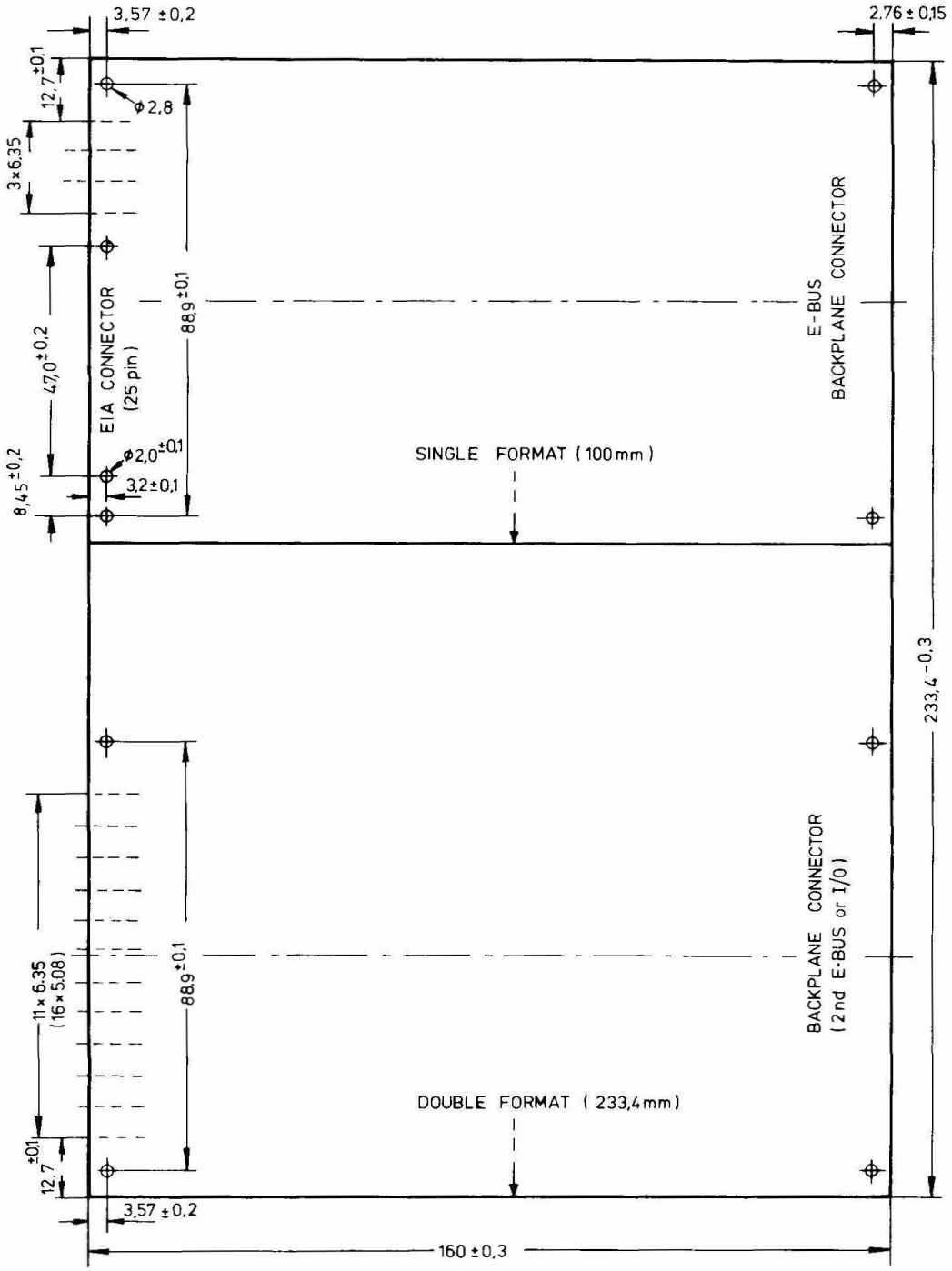


Figure 8-5 Peripheral Equipment Connector Locations

PIN	SIGNAL	INPUT/OUTPUT	DESCRIPTION
1	FRAME GND	-	Chassis Ground (Optional)
2	RCV DATA	INPUT	Serial Data In
3	XMT DATA	Output	Serial Data Out
4	(Not Used)		
5	CTS	Output	Clear To Send (To Terminal)
6	DSR	Output	Data Set Ready (To Terminal)
7	EIA GND	-	Signal Ground
8	DCD/RTS	Output	Data Carrier Detect (To Terminal)/ Request to send (to Modem)
9-11	(Not Used)		
12*	+12 VOLTS	Output	+12 Volts for Microterminal
13*	-12 VOLTS	Output	-12 Volts for Microterminal
14*	+5 VOLTS	Output	+5 Volts for Microterminal
15	XMT CLK	Input	Transmit Clock
16*	CTS/RESTART	Input	Clear To Send (From Modem)/Load Interrupt From Microterminal
17	RCV CLK	Input	Receive Clock
18*	TTY RCV/+/INPULL	Input	TTY Receive/Multidrop Input Line
19	DSR	Input	Data Set Ready (From Modem)
20	DTR/DCD	Input/Input	Data Terminal Ready (From Terminal)/ Data Carrier Detect (From Modem)
21	DTR	Output	Data Terminal Ready (To Modem)
22	RNG	Input	Ring Indicator
23*	TTY RCV-/INPUSH	Input	TTY Receive/Multidrop Input Line
24*	TTY XMT-/OUTPUSH	Output	TTY Transmit/Multidrop Output Line
25*	TTY XMT+/OUTPULL	Output	TTY Transmit/Multidrop Output Line

+ TTY connections * microterminal connections

Table 8-4 RS-232-C/TTY Connector Pin Out In E-Systems

Note that for connection to equipment with an IEC bus, the alternative connector form is used, in contrast to the RS-232-C interface. Thus the possibility of interchange, which could lead to component damage, is eliminated. Table 8-5 shows the 25 pin equipment connector pin out corresponding to the European IEC standard.

PIN	SIGNAL	DESCRIPTION
1	DIO1	Data I/O-Line
2	DIO2	Data I/O-Line
3	DIO3	Data I/O-Line
4	DIO4	Data I/O-Line
5	REN	Remote enable
6	EOI	End or identify
7	DAV	Data valid
8	NRFD	Not ready for data
9	NDAC	Not data accepted
10	IFC	Interface clear
11	SRQ	Service request
12	ATN	Attention
13	SHIELD	Cable shield
14	DIO5	Data I/O-line
15	DIO6	Data I/O-line
16	DIO7	Data I/O-line
17	DIO8	Data I/O-line
18	Not used	
19-22	GND	logic ground
23	Not used	
24-25	GND	logic ground

Table 8-5 Pin Out of IEC Bus Equipment Connector

8.3 FRONT PANEL AND CHECK LENGTH

Front panels are optionally available for E-modules. They may be used to mount connectors, display, and servicing devices, and/or produce an acceptable cosmetic or safety effect for table-top equipment.

8.3.1 MOUNTING OF DISPLAY DEVICES

Display devices can be mounted directly in the front panel and must have a vertical spacing of 6.35mm or 5.08mm. In modules which only have a front panel as an optional extra display devices should utilise a mounting block (Dialight series 550 or similar).

Fig.8-6 shows an LED mounting block with the correct vertical spacing. As a check measurement, the distance from the front panel to the back plane connector and to the back plane itself should be 169.93 +/- 0.4mm and 175.24 -0.14mm, respectively (to DIN 41949, part 5). The location of display devices on double Eurocards is shown in fig. 8-7. It should be noted that the mounting array starts 12.7mm from the upper or lower card edge.

LEDs used with a mounting block have a spacing of 6.35mm, and thus a maximum of 11 or 2 x 11 LEDs can be accommodated. If LEDs are used without mounting blocks, a maximum of 16 or 2 x 16 LEDs can be arranged with a spacing of 5.08mm (see fig.8-7).

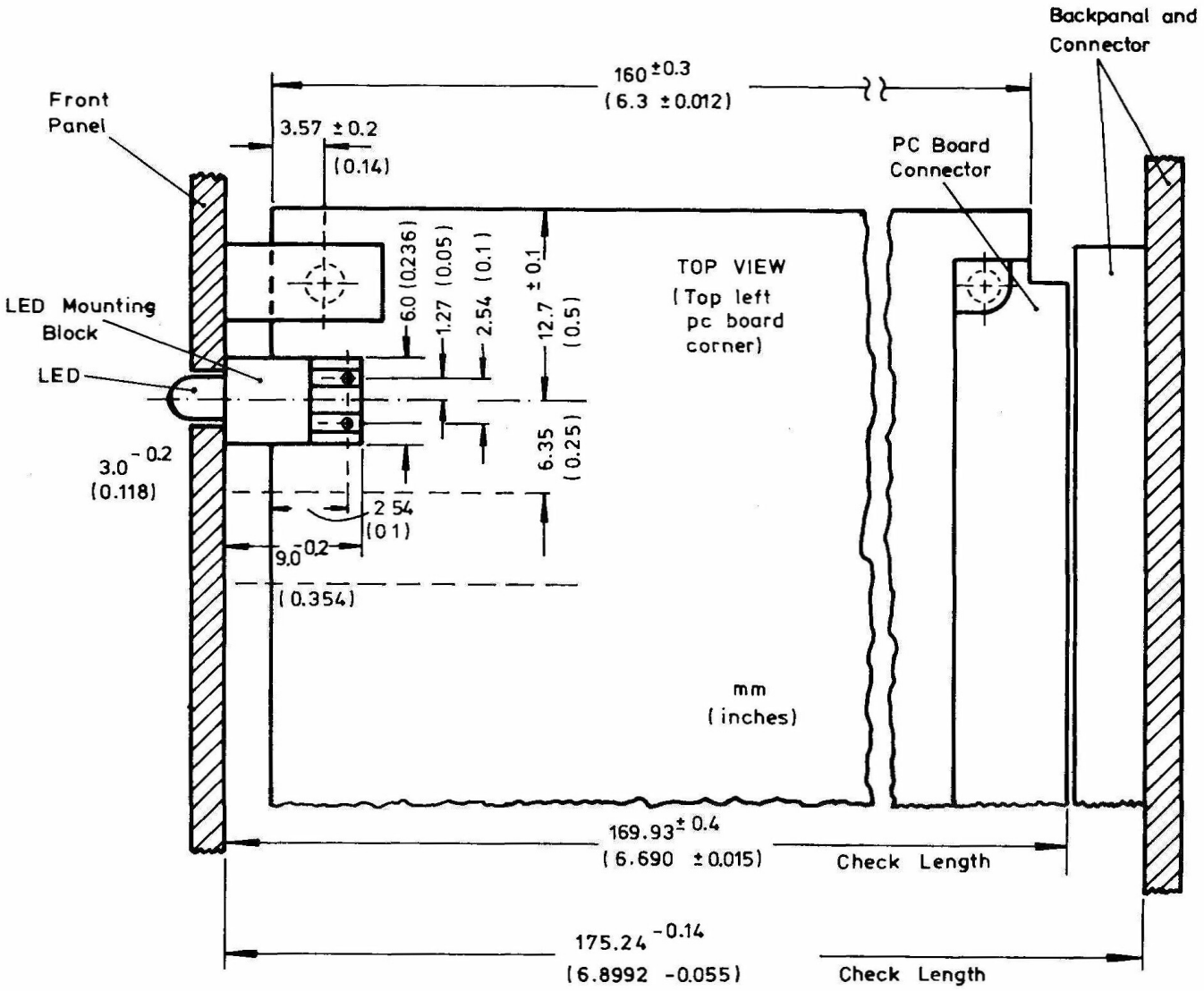


Figure 8-6 LED Mounting Block with 6.35mm Spacing

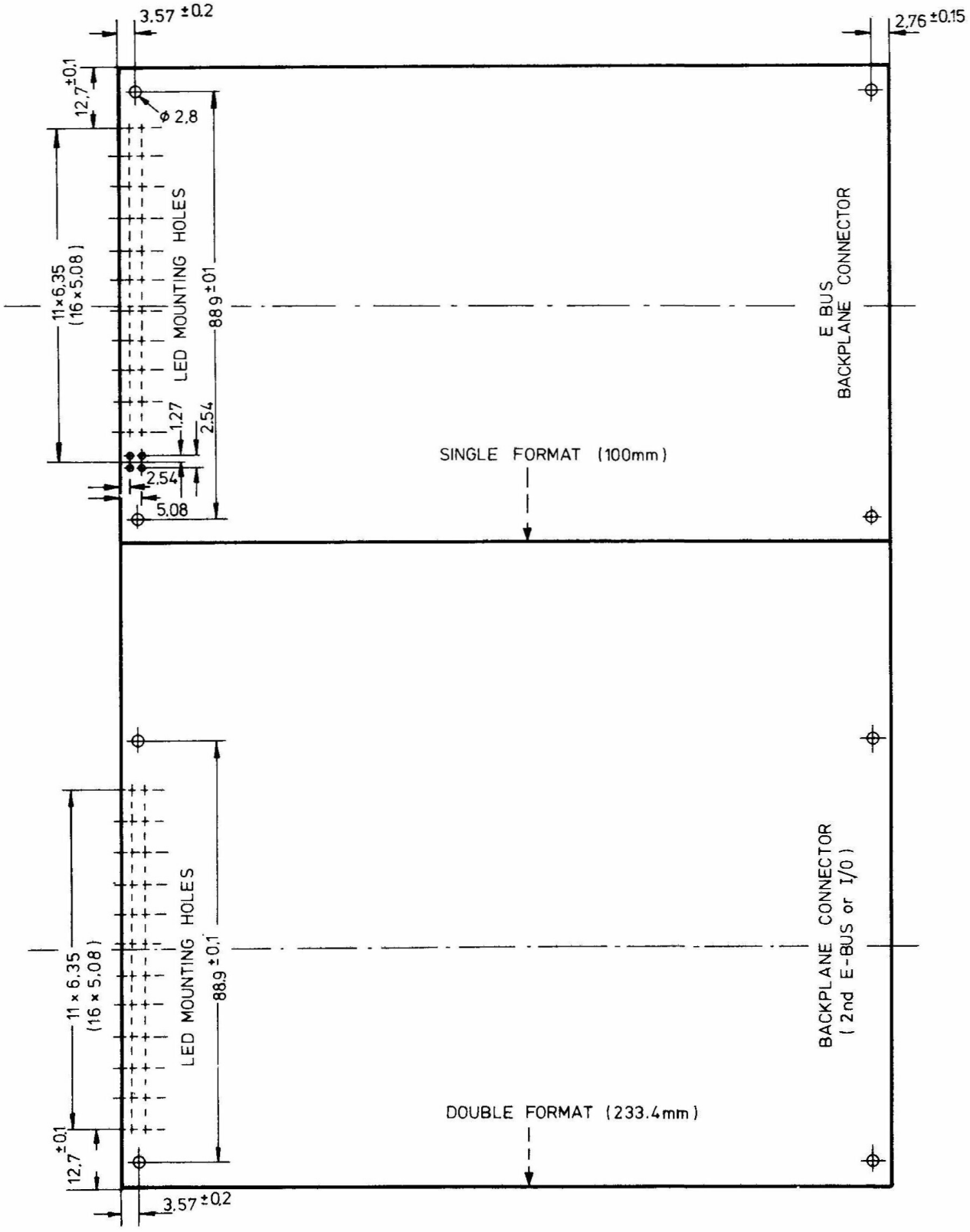


Figure 8-7 Spacing of Display Elements

8.3.2 FRONT PANEL DIMENSIONS

The standard width of the front panel is 4TE (20.32mm). For modules having tall components and/or protruding track side pins (e.g. WIRE- WRAP boards) an 8TE (40.64mm) front panel can also be provided. When constructing special modules for an E-System chassis (e.g. board pair) or a small peripheral unit (e.g. digital cassette station) the front panel should be a multiple of 4TE. The module then becomes a plug in unit for insertion in the chassis.

Fig.8-8 shows the dimensions and mounting of a single Eurocard front panel. The dimensions A and B for the front panel for a single and double Eurocard are:

Dimension	Single Format	Double Format
A	122.5 +/-0.2mm	255.85 +/-0.2mm
B	128.7 -0.3mm	262.05 -0.3mm

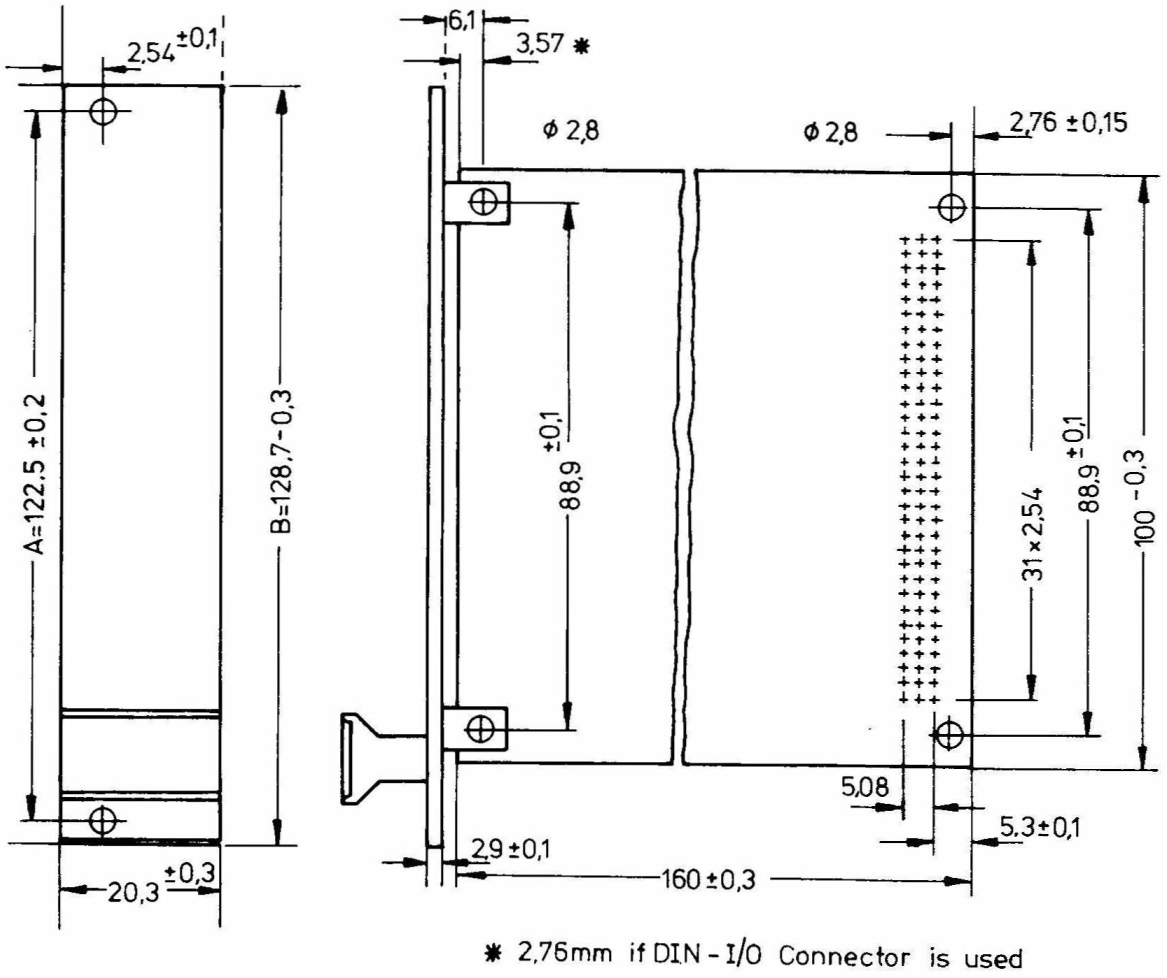


Figure 8-8 Single Eurocard Front Panel Dimensions

8.4 RACK MOUNTING CHASSIS

In addition to table-top chassis, E-modules may be housed in chassis intended for rack mounting. Of the numerous card and module housing systems available, only rack mounting chassis conforming to the DIN 41494 standard should be used in E-Systems. The position of the fixing holes and the mechanical design of modules for a 19" chassis are shown in fig.8-9. Separation of the front panel fixing holes is the same as those for the back plane, i.e. 122.5mm (5.08mm unit spacing). The distance from the back plane to the front panel inner edge should be 175.24mm as specified in DIN 41494, part 5.

For table-top chassis it should be noted that the front panel fixing holes on some types available on the market do not have the required separation of 122.5mm.

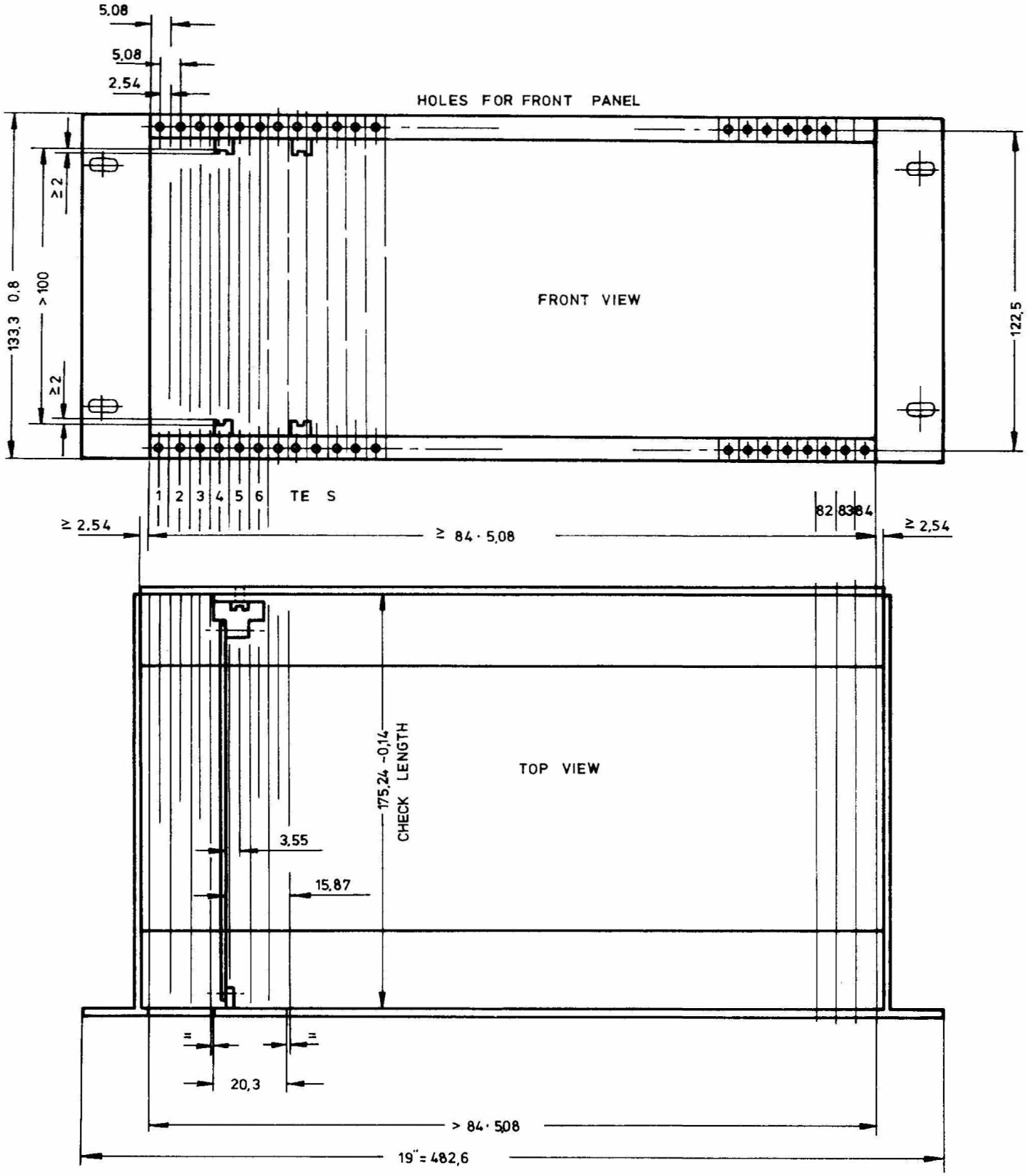


Figure 8-9 19" Chassis Dimensions

8.5 MAINS SUPPLY

Mains supplies for E systems must fulfill the special requirements in respect to the signals PWRFAIL- and PRES- (see section 2.3.4).

These requirements are detailed in the specification "Functional and Electrical Specification of Power Supplies for the TM990 and TM990/E Microcomputer Boards" which relate to a 36TE wide plug-in unit (3HE high).

SECTION 9

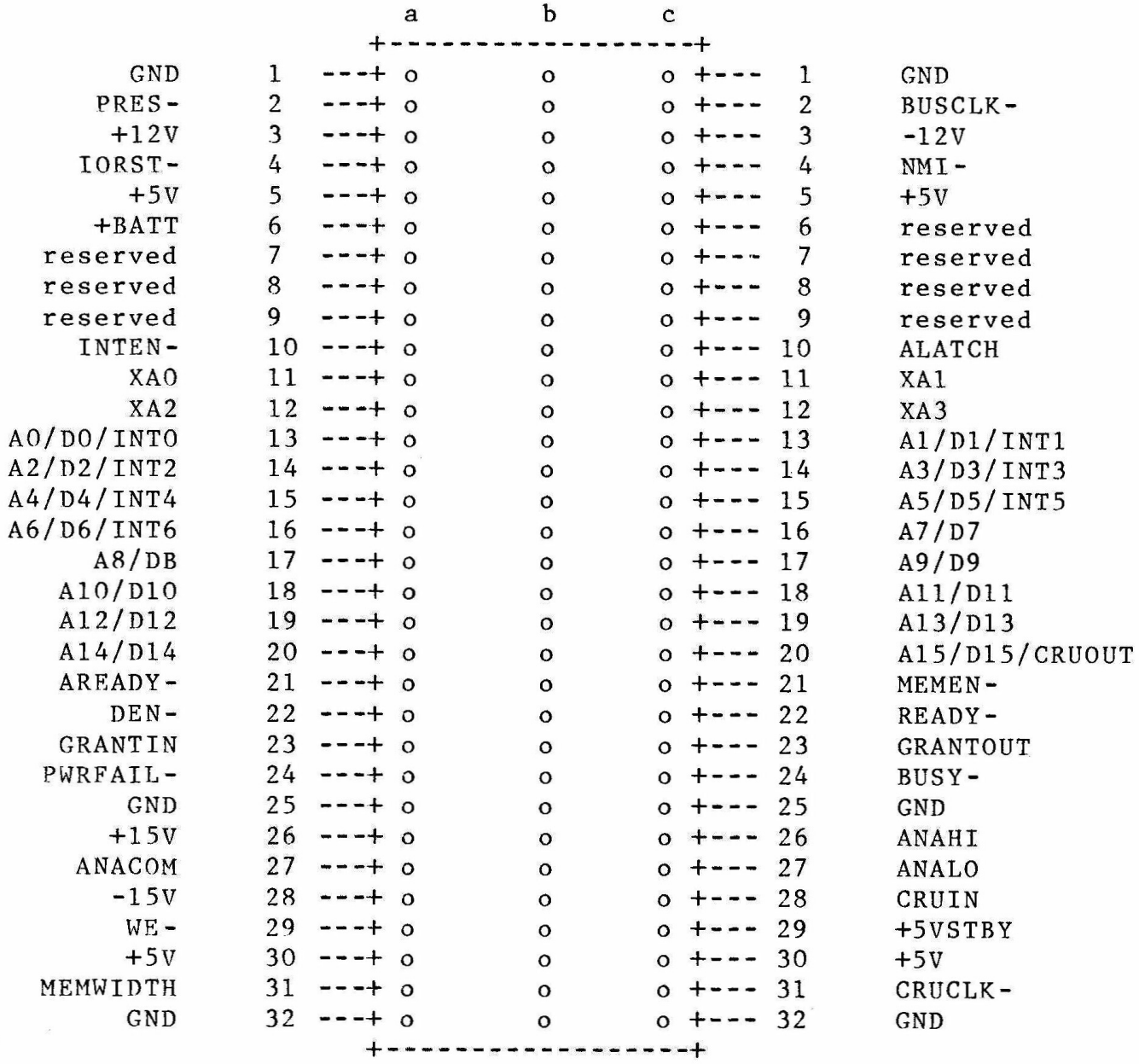
SUMMARY

This handbook is designed to explain to the user possible functions and applications of E-BUS and also to aid the development of special E-BUS modules. For this purpose the handbook contains various different examples for memory, input/output, and interrupt interface circuits. Further information can be found in the publications listed in section 1.1.

The design check list contained in Appendix B gives valuable notes aimed at the verification of the correct design and development of E-BUS modules.

APPENDIX A

E-BUS PIN OUT



APPENDIX B

DESIGN CHECK LIST FOR E-BUS MODULES

B.1 MICROCOMPUTER MODULES

- Have the timing constraints of E-BUS been fulfilled (make a worst-case timing diagram!)?
- Do all the signal drivers have sufficient drive capability (see section 2.5.5)?
- Do the interrupt lines PRES-, NMI- and PWRFAIL- have the necessary priorities?
- Can PWRFAIL- be read?
- Is the interrupt logic transparent to the software (see section 6.5.2)?
- Are signal inputs loaded with no more than two UBLs (see section 2.5.6)?
- Does the GRANTIN line have a pull up resistor to Vcc?
- Has the standard CRU address map been used (see section 5.3.1)?
- Are system status indicators provided (RUN and IDLE is the recommended minimum)?
- Are bus driver conflicts eliminated on the ADI bus?
- Are CRU and memory address ranges fully decoded on the MC-module?
- Is a sufficiently long Power-On-Reset provided, which operates on momentary supply voltage interruptions?

B.2 MULTI-MICROCOMPUTER MODULES

In addition to the points given for MC-modules the following should also be checked.

- Do the signal loading and driver capabilities correspond to the requirements of an MMC-system (48mA drive capability)?
- Is sufficient local memory provided so that bus loading is not too high?
- Is the MMC-module address decoded from the interrupt code?
- Is synchronisation between local clock and BUSCLK- provided?
- Is a bus lock generated for semaphore test (see section 3.5.3)?
- Are BUSCLK- and IORST- deselectable by a jumper (see section 3.3) ?
- Is parallel bus priority control planned (see section 3.2.2)?

B.3 MEMORY EXPANSION MODULES

- Do the signal loading and driver capabilities correspond to the E-BUS guidelines (see section 2.5.6)?
- Are the timing requirements of READY-/AREADY- fulfilled? (see section 4.4)
- Is an 8 and 16 bit data bus interface provided?
- Is data bus conflict completely avoided (see section 4.2.3)?

- Are A15 and MEMWIDTH decoded on parallel input/output modules, and is a READY- signal generated (see section 4.5)?

- Can the address space be relocated across the 1M byte address range in maximum 2k steps for modules with less then 16 k byte or in maximum 4k byte steps for modules with above 16 k byte capacity?

- Is the address decoding sufficiently flexible (see section 4.3)?

- Are the E-BUS pins GRANTIN and GRANTOUT joined?

- Is the capacity of a back up battery sufficient for a minimum of 72 hours operation and are WE- and CS- inhibited during power up and down (see section 4.7)?

B.4 INPUT/OUTPUT MODULES

- Is the utilised CRU address range fully decoded?

- Has sufficient decoding flexibility been allowed?

- Is sufficient test capability in hardware provided (through MC-module software) ?

- Are all I/O ports reset with IORST-?

- Are the GRANTIN and GRANTOUT pins joined when no interrupt is to be generated?

- Do the signal loading and driver capabilities correspond to the E-BUS guidelines? (see section 2.5.6)?

- Are the I/O ports resettable using a software command?

- Is polarisation of the E-BUS and I/O connectors provided on a single Eurocard?

B.5 INTERRUPT MODULES

- Are all interrupt sources reset by IORST?
- Are all interrupt sources resettable or maskable by I/O command?
- Are bus requests synchronised with BUSCLK- and the necessary timing requirements met (see section 6.4)?
- Is the transmission of the interrupt code repeated until the interrupt source is reset?
- Is INTEN- usable as a common interrupt request line (open collector output !, see section 6.8)?
- Can the interrupt channels be triggered/tested by software?
- Is GRANTIN provided with a pull up resistor to Vcc?
- Should the module be controllable by several MMC-modules ? (If yes, the interrupt code should be software programmable, see section 7.3)
- Is the maximum time delay from GRANTIN to GRANTOUT achieved ? (see section 3.2.1)
- Is parallel bus priority control possible (see section 3.2.2)?

B.6 BACK PLANE WIRING

- Does the back plane correspond to the E-BUS guidelines (see section 2.5.4)?
- Does the line termination meet the E-BUS guidelines (see section 2.5.3)?
- Is a SENSE connection required for the +5V?

- Are GRANTIN/OUT jumpers provided?

- Are there connections to the mains supply for PWRFAIL-, PRES- and +5VSTBY?

B.7 MAINS SUPPLY

- Does the mains supply fulfill all the E-System requirements (PWRFAIL-, PRES- generation, see section 8.5)?

- Are the current ratings of the supply adequate (note environmental temperature!, see section 2.5.6)?

- Have limit condition tests been performed?

B.8 GENERAL DESIGN RULES FOR E-BUS MODULES

It is recommended that the following general design rules for E-BUS modules be followed:

- Provide as much software test capability in hardware as possible!

- Error or function indicators should be built in, as far as possible!

- Select universal and flexible decoding!

- The maximum power dissipation on a single Eurocard is 12W per module (without special cooling)!

- In MMC systems, minimise E-BUS loading per module.

- As far as possible, implement functional distribution into individual modules.

- Develop memory modules with 8 and 16 bit interfaces wherever possible.

- Couple intelligent control units loosely to the E-BUS (e.g. Dual-Port-Memory).

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