Microprocessor Engineering Limited
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0703-780084

MPE FD/WD-E - User Manual

Rev 1.0
October 1984

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E-bus Floppy & Winchester Disc Controller

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1. Introduction

The MPE FD/WD-E card interfaces the E-bus to Western Digital's WD-1002 series of floppy and hard disc controllers. These controllers can support four floppy disc drives and three Winchester disc drives with ST506 interfacing. Support for floppy discs only is available via MPE's forthcoming FD-E card.

2. Installation and Configuration

The card should be linked for the required memory address (MPE standard is 00.FF00), and then installed. The 40-pin ribbon cable should be taken to the host adapter connector on the WD-1002 card. This card has the same form factor and mounting holes as a standard 5" floppy disc unit, and so may be mounted on the drive. Power to the WD-1000 should be supplied separately.

The card is capable of generating a memory overlay signal, PHANTOM-, which MPE's memory cards can respond to. This signal disables memory on these other cards, so allowing only the space required for the interface to be lost.

2.1. Linking

Link	Function
1,2	not used
3	fit to enable INTREQ to INTEN- on E-bus
4	fit to enable DRQ to INTEN- on E-bus
5,9,10	not used
11	fit to enable FD/WD-E to generate PHANTOM-
12	fit to use E-bus AREADY- line (9900 only)
13	fit to use E-bus READY- line (9995 & 99000)
Int. Lev.	
0	spare - no interrupts generated
1	interrupt generated on PWRFAIL-
4	interrupt generated on INTEN-
Waits	
1	0 wait states
2	1 " "

3	2	"	"	(default for 3MHz 9995)
4	3	"	"	
5	4	"	"	
6	5	"	"	
7	6	"	"	

2.2. Address selection

The two DIL switches are used to select the required base address. MPE software uses 00.FF00 as a default, with PHANTOM- being generated to overlay the RAM-E card(s).

Switch	Address line (open=1)
SW1/1	XA0
SW1/2	XA1
SW1/3	XA2
SW1/4	XA3
SW1/5	A0
SW1/6	A1
SW1/7	A2
SW1/8	A3
SW2/1	A4
SW2/2	A5
SW2/3	A6
SW2/4	A7
SW2/5	A8
SW2/6	A9
SW2/7	A10
SW2/8	not used

3. Software

Sample software listings for a device driver are included at the rear of the manual. The listing shown is for a simple non-interrupt driven handler for the MDEX operating system.

The card occupies a 32 byte slot. Because of the requirements of 9900 and 9980/81 processors, which perform a read before a write, and the software constraints of the WD-1002 cards, it has been arranged that offsets 0-15 generate read accesses to the WD card, and 16-31 generate write requests. A15 is ignored. In 16-bit systems data will be transferred on the low byte of of the data bus (AD8-15). System software that has to be independent of processor type and data bus width should access the card by byte transfers on odd addresses.

4. Theory of operation

How the card works is discussed in three sections, address decode logic, wait state generation, and WD-1002 drive logic.

4.1. Address decode logic

Memory addresses are captured from the E-bus by two latches (IC 10 and 11), and applied to two linked octal comparators qualified by MEMEN-.

The required address is set up on the two DIL switches, SW1 and SW2. The enable output of the comparators is then fed to the wait state logic, the WD-1002, and the data bus buffers.

4.2. Wait state logic

The inverted enable signal is fed to the shift register (IC9, 74LS164) inputs and the PHANTOM- generator. The shift registor ouput is inverted and used as READY- or AREADY-. The shift register is cleared by ALATCH-.

4.3. WD-1002 driver logic

The data bus is buffered by a 74LS245 (IC7). Three latched address lines, AD12, AD13, and AD14, become the WD cards A2, A1, and A0 respectively. The WD-1002 control strobes, RE- or WE-, are generated and delayed slightly, for a true address decode and ALATCH low. A read strobe is generated for AD11 low, DEN- active (low), and WE- inactive (high). Conversely, a write strobe is generated for AD11 high, DEN- inactive (high), and WE- active (low). This arrangement prevents the FD/WD-E from accessing the WD card during the read cycle immediately before a write that is generated by 9900 and 9980/1 processors for any writes, and by 99000 processors during byte writes. The WD RESET- signal is a buffered version of the E-bus IORST- signal.

5. Connector

The connector to the WD card is a 40-way IDC connector. All the even numbered pins (2-40) are grounded.

Pin	Function
2-40	grounded
1	D0 (lsb)
3	D1
5	D2
7	D3
9	D4
11	D5
13	D6
15	D7 (msb)
17	A0 (lsb)
19	A1
21	A2 (msb)
23	ENABLE-
25	WE-
27	RE-
29,31,33	not used
35	INTREQ
37	DRQ
39	RESET-

6. Ebus pin-out

For full details of E-bus use and specification, see the 'E-bus System Design Handbook' published by Texas Instruments European Semiconductor Group, September 1981, TI part number MP402.

Ident - Row A	Row A	Row C - Ident
Gnd	1	Gnd
PRES-	2	BUSCLK-
+12v	3	12v
IORST-	4	NMI-
+5v	5	5v
+BATT	6	reserved *1
reserved	7	reserved
reserved	8	reserved
reserved	9	reserved
INTEN-	10	ALATCH
XA0	11	XA1
XA2	12	XA3
A0/D0/INT0	13	A1/D1/INT1
A2/D2/INT2	14	A3/D3/INT3
A4/D4/INT4	15	A5/D5/INT5
A6/D6/INT6	16	A7/D7
A8/D8	17	A9/D9
A10/D10	18	A11/D11
A12/D12	19	A13/D13
A14/D14	20	A15/D15/CRUOUT
AREADY-	21	MEMEN-
DEN-	22	READY-
GRANTIN	23	GRANTOUT
PWRFAIL-	24	BUSY-
GND	25	GND
+15V	26	ANAHI
ANACOM	27	ANALO
-15V	28	CRUIN
WE-	29	+5vSTBY
+5v	30	+5v
MEMWIDTH	31	CRUCLK-
GND	32	GND

*1 6C is optionally redefined on some MPE cards (FD/WD-E and RAM-E) as PHANTOM-. This is an open collector signal terminated on the backplane that may be pulled low by any memory-mapped peripheral wanting to overlay memory. The memory card that that responds to this signal should treat it as an inhibit signal and, as a minimum, should disable its data bus buffers, and should not activate READY-. PHANTOM- should be asserted as soon as possible in a memory cycle. Use of this facility is made in systems where it is desired to have as much memory as possible, losing only the minimum possible space to memory-mapped peripherals. To take full advantage of this feature, we suggest that memory mapped peripherals be positioned at or above OFF00.

FD/WD-E Manual
Rev 1.0

Normal setting
address = FF00
links 4 waits
links 3
int level 4
11
13

FD/WD-E

NB. Solder side and track-side cuts !

1/ Cut track to IC10 pin 11

Connect IC10 pin 11 to BUS C10

2/ Cut track IC4 pin 10 to link block 6

link IC4 pin 12 to link block 6

link IC4 pin 10 to BUS A8

Add 220R from IC4 pin 10 to IC4 pin 14

3/ Add 470R from IC4 pin 6 to IC4 pin 14

4/ IC5 MUST be HC14

Cut track (top-side) to IC5 pin 4

Cut track to P2/25

LINK IC5 pin 8 to P2/25

link IC5 pin 9 to IC5 pin 10

Add 2k2 from IC5 pin 11 to +5v at IC5 pin 14

Add 330 pf from IC5 pin 4 to IC5 pin 11

5/ Cut top-side track to IC9 pin 2

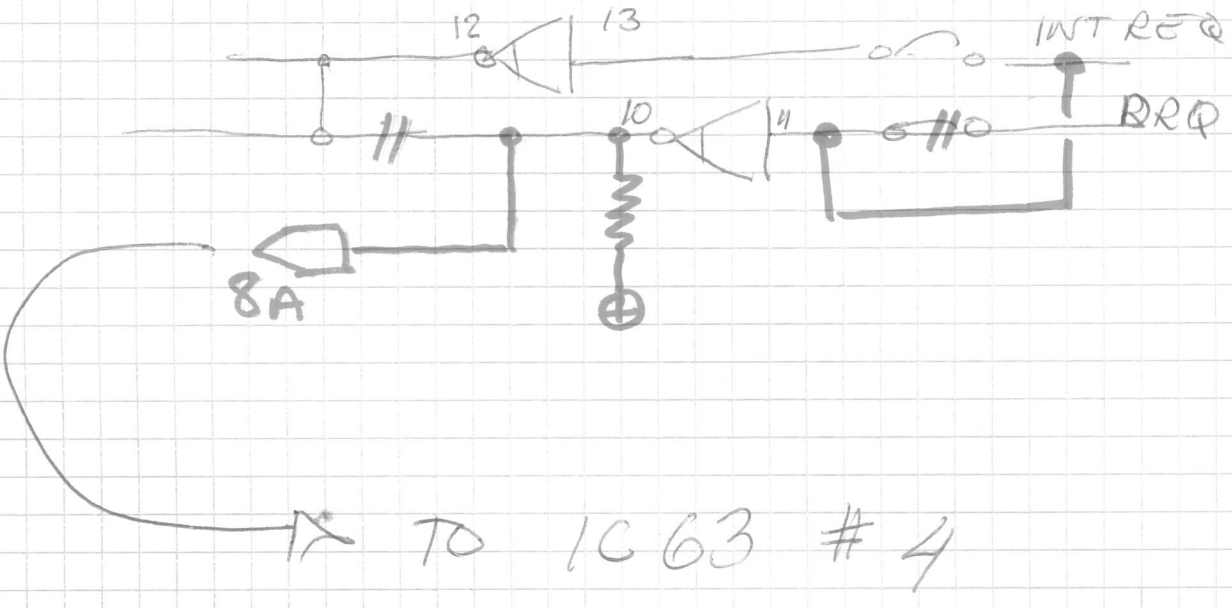
link IC9 pin 2 to IC5 pin 13

6/ check against circuit diagrams.

MPE - FD/WD - E ISS A

QTY	PART NO	CCT REF
1	74S05	IC4
1	74LS14	IC5
1	74LS138	IC3
1	74LS164	IC2
2	74LS245	IC6,7
2	74LS373	IC10,11
2	74LS688 (OR Am25LS2521)	IC8,9
2	SWITCH 8WAY DIL	SW1,2
2	RESISTOR 1K	R1,2
2	RESISTOR N/W 9x10K	RP1,2
2	CAPACITOR 10µF 16V TANT	C1,2
7	CAPACITOR 0,01µF CER.	C2,4,'C'
1	" 3n3	C6
1	" 5n6	C5
2	20 PIN PLUG	
A/R	SHORTING JUMPERS	
1	64 PIN RT-ANGLE PLUG DIN 41612C	

MPE FD/WD-E



TO IC63 #4

AS ON PP95

FD/WD-E links

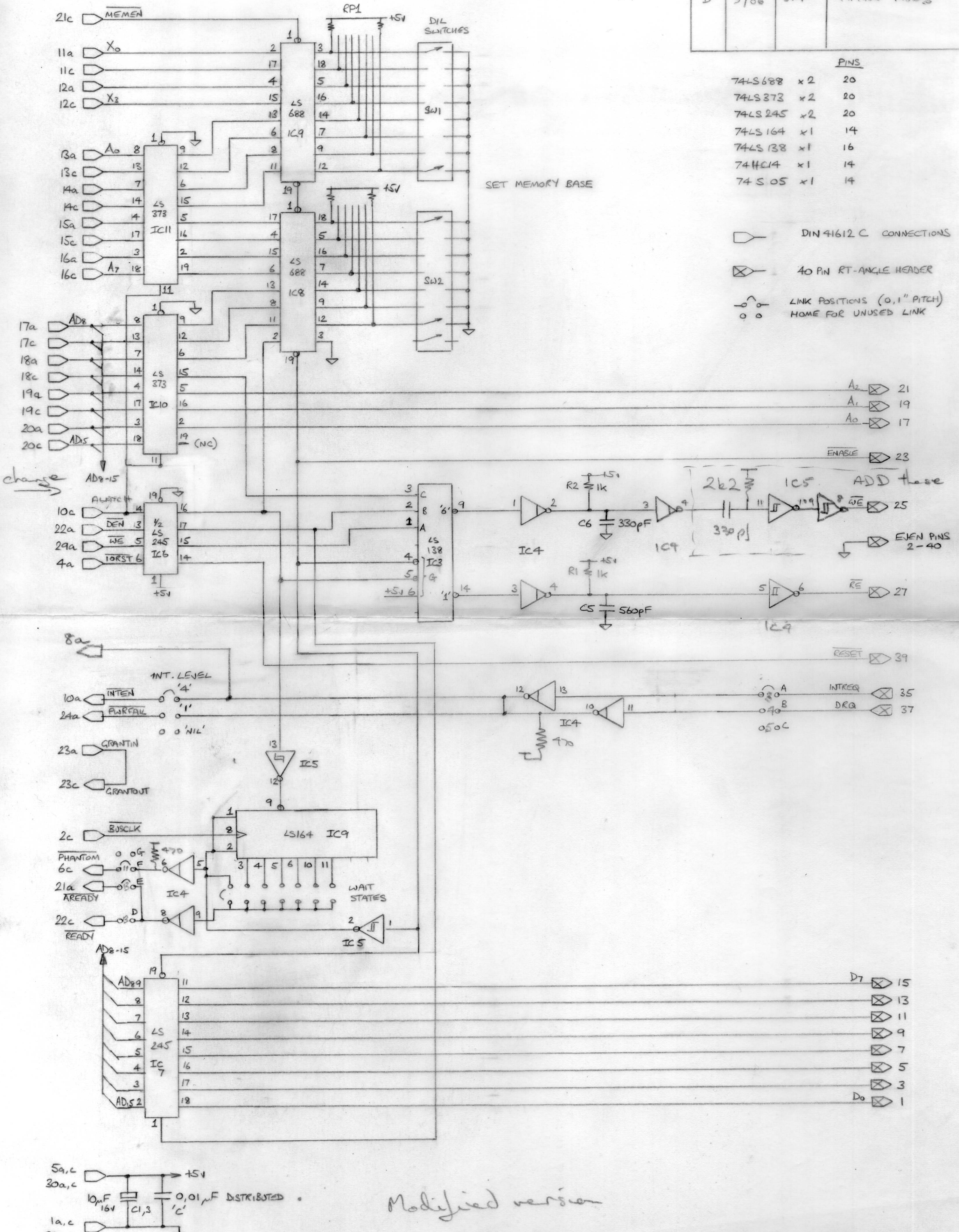
1	NU
2	NU
3	A — INTREQ
4	B — DRQ
5	NU
9	NU
10	NU
11	F — PHANTOM
12	E — AREADY
13	D — READY

```
SRATE = 8 .. STEP RATE
BUFFER = >1800                ..SECTOR BUFFER START ADDR
SCODE = 0                     ..SECTOR SIZE CODE
DRIVE = 0
SIDE = 0                      ..
NSEC = 16                     .. NO OF SECTORS FOR FORMAT
DRQ  = 8                      .. DATA REQUEST BIT
READ$ = 1
WRITE$= 2
INIT$ = >80

DELE('STATUS','H','READIT','WRITIT','RD','WT','FMAT')

FUNC STATUS(0,2)              ..READ STATUS
  CRUB=>400
  CRUW(28,1,1)
  LOC 2 = 0
  REPEAT
    BEGIN
    LOC 1 = @>E0CE
    END
  UNTIL ((LOC 1 AND >8000) EQ 0)
  RETURN LOC 1 >> 8
  END

PROC H(0,1)                   ..HOME HEAD ON DRIVE
  LOC 1=>1800 + ((SCODE AND 3)<<13) + ((SIDE AND 1) << 8)
  LOC 1=LOC 1 + ((DRIVE AND 3)<<9)
  @>E0DC = LOC 1                  .. SET DRIVE
  @>E0DE = >1000 + (SRATE << 8)          .. ISSUE COMMAND
  STATUS
  END

PROC READIT(0,2)              ..READ DATA INTO BUFFER
  FOR LOC 1 = 0 TO 255 DO
    BEGIN
    IF LOC 1 MOD 2 EQ 0 THEN
      LOC 2 = @>E0C0 AND >FF00
    ELSE
      BEGIN
      LOC 2 = LOC 2 OR (@>E0C0 >> 8)
      @(BUFFER + LOC 1) = LOC 2
      END
    END
  'SECTOR COUNT  = ';@>E0C4 >> 8;NL
  'SECTOR NUMBER = ';@>E0C6 >> 8;NL
  'TRACK  NUMBER = ';@>E0C8 >> 8;NL
  IF (STATUS AND 8) NE 0 THEN 'MORE DATA TO FOLLOW'
  END

PROC WRITIT(0,2)              ..WRITE DATA FROM BUFFER
  FOR LOC 1 = 0 TO 255 DO
    BEGIN
    IF LOC 1 MOD 2 EQ 0 THEN
      @>E0D0 = @(BUFFER + LOC 1)
    ELSE
      @>E0D0 = @(BUFFER + LOC 1 -1 )<<8
    END
  STATUS
  'SECTOR COUNT  = ';@>E0C4 >> 8;NL
  'SECTOR NUMBER = ';@>E0C6 >> 8;NL
  'TRACK  NUMBER = ';@>E0C8 >> 8;NL
```

```
   IF (STATUS AND 8) NE 0 THEN 'MORE DATA REQUIRED'
   END

PROC RD(0,1)                    ..READ (TRACK,SECTOR,[COUNT])
   IF ARG 0 NE 0 THEN
     BEGIN
     @>EOD8 = ARG 1 << 8
     @>EOD6 = ARG 2 << 8
     END
   IF ARG 0 EQ 3 THEN
     BEGIN
     @>EOD4 = ARG 3<<8
     @>EODE = >2400             ..READ MULTIPLE
     END
   ELSE
     BEGIN
     @>EOD4 = >100                ..SET 1 SECTOR
     @>EODE = >2000
     END
   IF (STATUS AND 1) EQ 0 THEN
     READIT
   ELSE
     BEGIN
     'ERROR CODE ';@>EOC2 >> 8:H2
     END
   END

PROC WT(0,1)                    ..WRITE (TRACK,SECTOR,[COUNT])
   IF ARG 0 NE 0 THEN
     BEGIN
     @>EOD8 = ARG 1 << 8
     @>EOD6 = ARG 2 << 8
     END
   IF ARG 0 EQ 3 THEN
     BEGIN
     @>EOD4 = ARG 3<<8
     @>EODE = >3400             ..WRITE MULTIPLE
     END
   ELSE
     BEGIN
     @>EOD4 = >100                ..SET 1 SECTOR
     @>EODE = >3000
     END
   IF (STATUS AND 1) EQ 0 THEN
     WRITIT
   ELSE
     BEGIN
     'ERROR CODE ';@>EOC2 >> 8:H2
     END
   END

PROC FMAT(1,3)                  ..FORMAT (TRACK NO)
   ARG 1 = ARG 1<<8
   LOC 1=NSEC<<8
   @>EOD4 = LOC 1               ..SECTOR COUNT
   @>EOD8 = ARG 1               ..TRACK NO
   @>EODE = >5000               ..ISSUE COMMAND
   STATUS
   LOC 1 = >100                 ..INIT SECTOR NO
   LOC 3 = 0
   REPEAT
     BEGIN
```

```
      @>EODO = 0
      @>EODO = LOC 1
      LOC 1 = LOC 1 + >100 ..NEXT SECTOR NO
      LOC 3=LOC 3+2
      END
    UNTIL LOC 1 GT NSEC << 8
    FOR LOC 1=LOC 3 TO 256 DO  @>EODO = 0
    STATUS
    END

DELE('CALL')
PROC CALL(1,0)              ..CALL( <func>,<trk>,<sec>,<mem>,<length> )
    WP = WD1002.STACK + >10
    R1 = ARG 1
    IF ARG 0 GT 1 THEN
      BEGIN
      R2 = ARG 2
      R4 = ARG 3
      R5 = ARG 4
      R6 = ARG 5
      END
    R8 = WD1002.UT$FD1
    R10 = WD1002.STACK
    R11 = WD1002.STACK + >30
    @R11 = £IDLE£
    PC = WD1002.PIOPSF
    TRUN;ERUN
    WHILE EST EQ 1 DO NULL
    IF EST EQ 3 THEN
      BEGIN
      EHLT
      R1
      IF R1 NE 0 THEN R2
      END
    ELSE
      'BKPT!'
    NL
    END
```

E-BUS WINCHESTER INTERFACE			
C	27/2/84	REDRAWN	
D	5/86	SFP	TIMING MODS



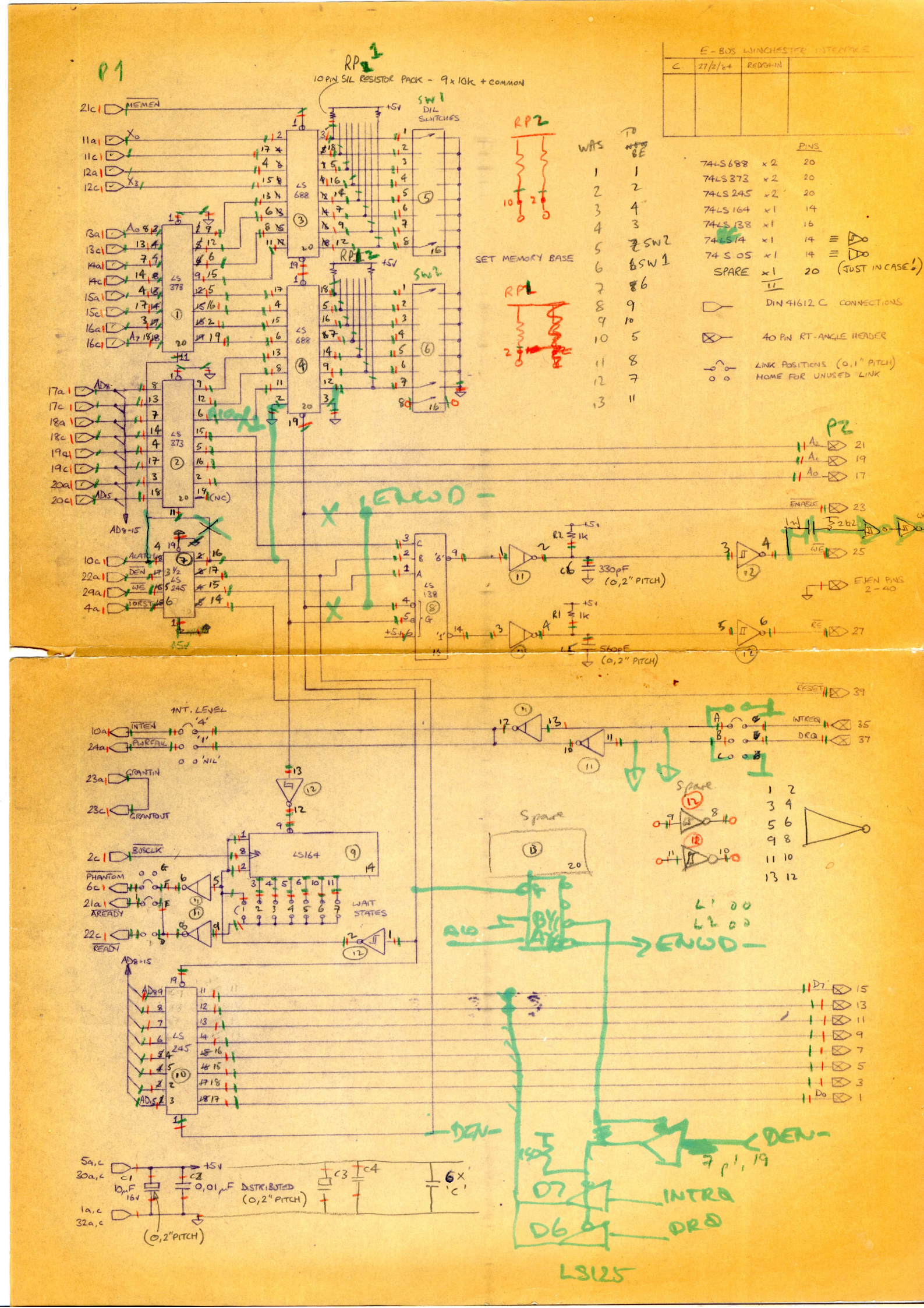
		PINS
74LS688	×2	20
74LS373	×2	20
74LS245	×2	20
74LS164	×1	14
74LS138	×1	16
74HC14	×1	14
74S05	×1	14

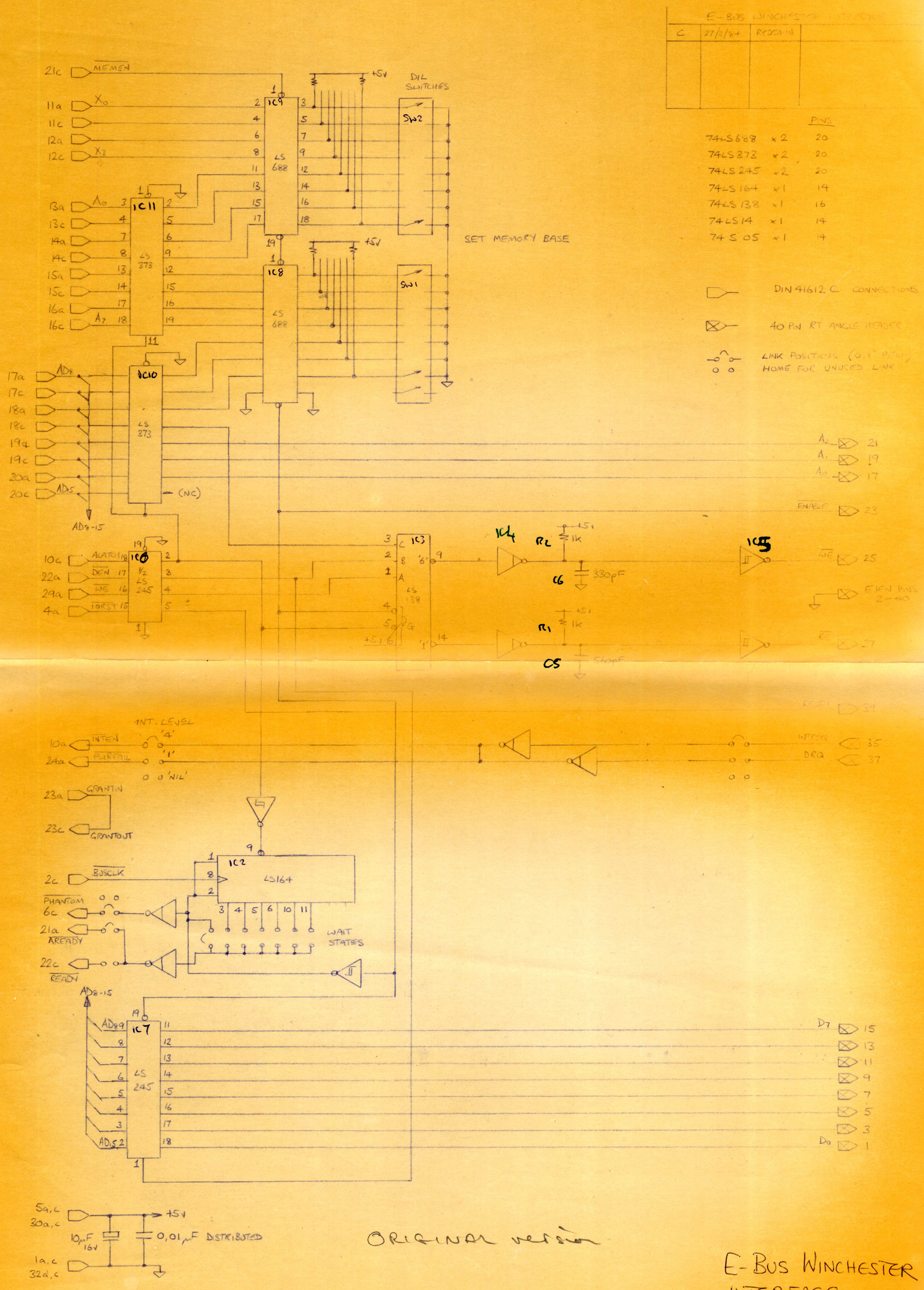
DIN 41612 C CONNECTIONS

40 PIN RT-ANGLE HEADER

LINK POSITIONS (0,1" PITCH)
HOME FOR UNUSED LINK

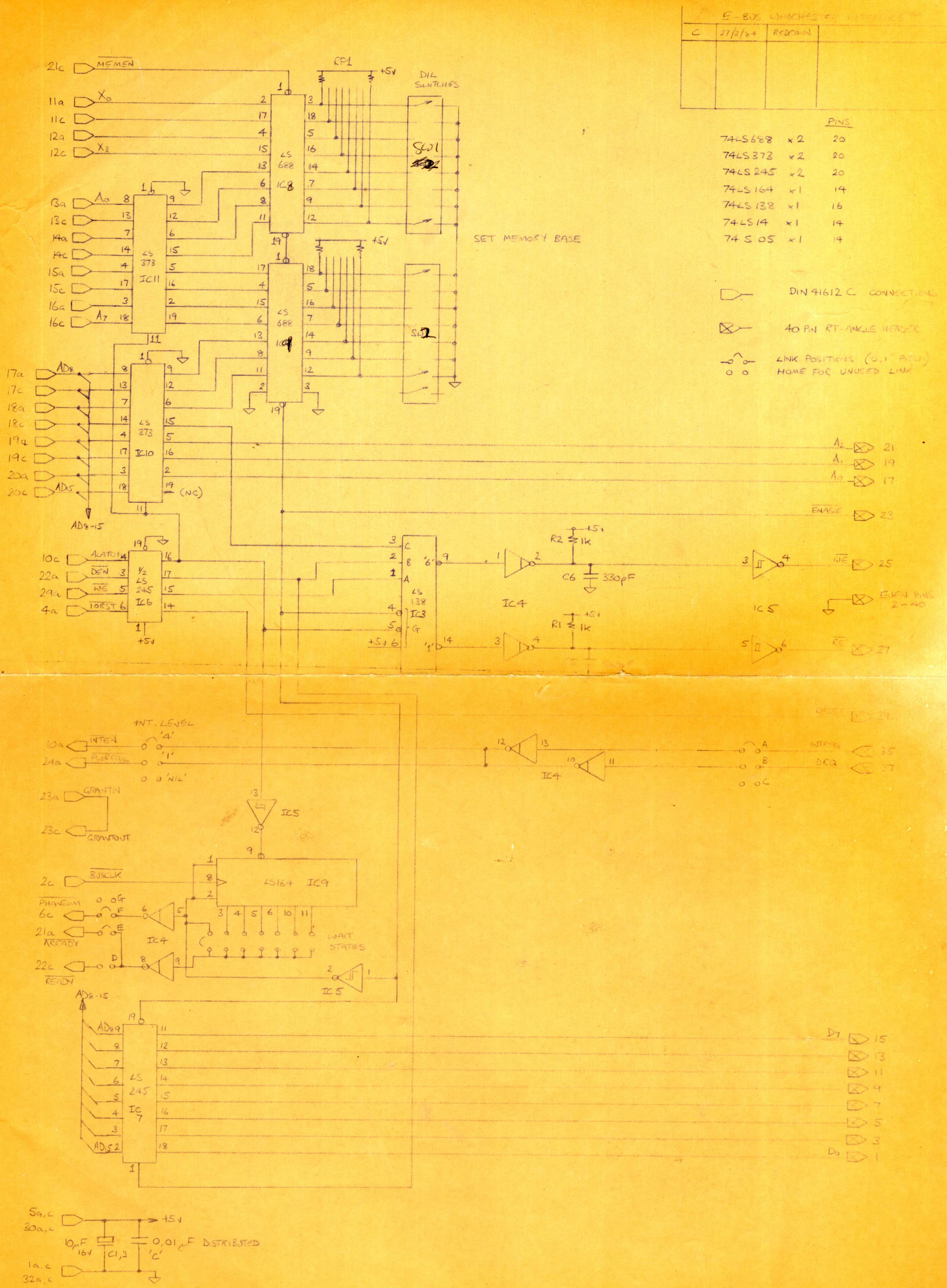
Modified version for WD 1002-05


P1
RP1
10 PIN SIL RESISTOR PACK - 9 x 10k + common
E-BUS WINCHESTER INTERFACE
C 27/2/84 REDRAWN
SW1 DIL SWITCHES
RP2
SET MEMORY BASE
RP1
WIRE TO BE
1 1
2 2
3 4
4 3
5 SW2
6 SW1
7 6
8 9
9 10
10 5
11 8
12 7
13 11
74LS688 x2 20
74LS373 x2 20
74LS245 x2 20
74LS164 x1 14
74LS138 x1 16
74LS14 x1 14
74S05 x1 14
SPARE x1 20
11
DIN 41612 C CONNECTIONS
40 PIN RT-ANGLE HEADER
LINK POSITIONS (0,1" PITCH)
HOME FOR UNUSED LINK
P2
ENWD-
ENABLE
WE
RE
EVEN PINS 2-40
330pF (0,2" PITCH)
560pF (0,2" PITCH)
INT. LEVEL
'A'
'1'
'NIL'
INTEN
PWRFAIL
GRANTIN
GRANTOUT
BUSCLK
PHANTOM
AREADY
READY
LS164
WAIT STATES
Spare
RESET
INTREQ
DRQ
BYP
ENWD-
DEN-
INTRQ
DRQ
LS125
DISTRIBUTED (0,2" PITCH)
10µF 16V
0,01µF
6x 'C'

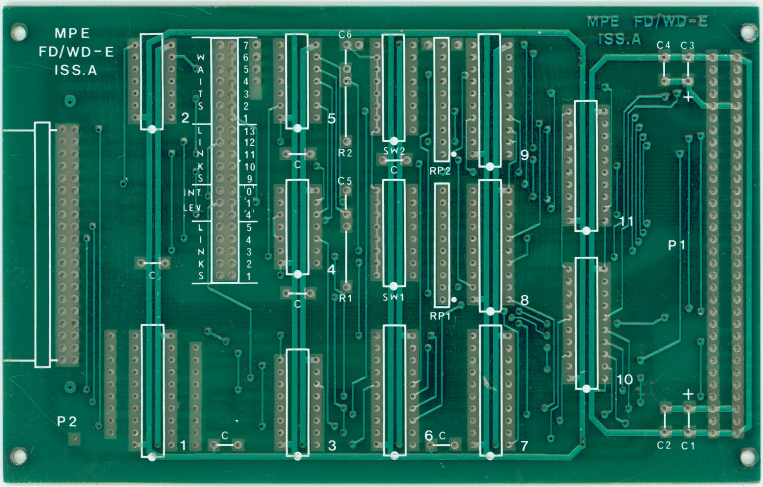


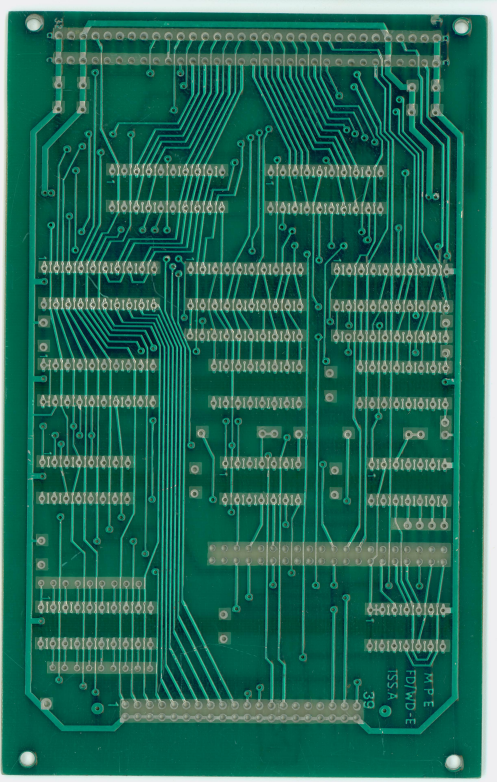
ORIGINAL version

E-BUS WINCHESTER INTERFACE



E-BUS WINCHESTER
C | 27/2/84 | REDRAWN
PINS
74LS688 ×2 20
74LS373 ×2 20
74LS245 ×2 20
74LS164 ×1 14
74LS138 ×1 16
74LS14 ×1 14
74S05 ×1 14
DIN 41612 C CONNECTIONS
40 PIN RT-ANGLE HEADER
LINK POSITIONS (0.1" PITCH)
HOME FOR UNUSED LINK
SET MEMORY BASE
DIL SWITCHES
RP1
+5V
SW1
SW2
MEMEN
LS 688 IC8
LS 688 IC9
LS 373 IC11
LS 373 IC10
½ LS 245 IC6
LS 138 IC3
IC4
IC5
LS164 IC9
LS 245 IC7
AD8-15
ALATCH
DEN
WE
IORST
ENABLE
R2 1K
C6 330pF
R1 1K
EVEN PINS 2-40
INT. LEVEL
'4'
'1'
'NIL'
INTEN
GRANTIN
GRANTOUT
INTREQ
DRQ
BUSCLK
PHANTOM
AREADY
READY
WAIT STATES
10µF 16V
C1,3
0,01µF DISTRIBUTED 'C'


MPE
FD/WD-E
ISS.A
MPE FD/WD-E
ISS.A
WAIT LINKS
INT LEV LINKS
7 6 5 4 3 2 1
13 12 11 10 9
0 1 4
5 4 3 2 1
C6
C5
R2
R1
SW2
SW1
RP2
RP1
C4 C3
C2 C1
P1
P2
1
2
3
4
5
6
7
8
9
10
11


MPE
PDMD-E
ISS A
39