Section 4 Microcomputer boards

TM990E/BUS

E-BUS MICROCOMPUTER

FEATURES:

- **Provides a standard electrical and mechanical connection.**
- **20 line address/data/interrupt bus.**
- **16 lines control bus.**
- **3 lines CRU bus (CRUOUT is multiplexed with A/D15).**
- **3 lines analog signal bus.**
- **7 lines reserved.**

DESCRIPTION:

Power Bus:- 4 lines for +5V, 1 line +12V, 1 line −12V, +BATT, +5VSTBY, +15V, −15V and 6 GND lines. These lines provide regulated voltages to the modules, +15V and −15V are for use by the analog interfaces, and there are 2 lines for backup, +5VSTBY which is used when the power fails and when it is operational, and a +BATT line which is for other than 5V and is only used in a powerfail mode.

Address/Data/Interrupt Bus:- Consists of 20 three state lines. These lines are triple multiplexed to function as address/data/interrupt buses at different points in time, A/D 15 is also used as a CRUOUT line. The particular type of data on the bus at a particular time is indicated by the control bus. This bus can only be driven by the present bus master. The address bus allows addressing up to 1MByte of memory using 16 basic address lines and 4 extended address lines, it also allows 12 bit CRU addressing. The data bus consists of 16 bi-directional lines. The interrupt bus consists of 7 lines which hold an interrupt code (consists of priority and who is to service) when an interrupt has occurred (signaled by INTEN line going to logic 0).

Control Bus:- This consists of 16 lines which control all transactions on the bus, it can be broken down into several subsets:-

Memory Control:- Consists of $\overline{\text{MEMEN}}$, $\overline{\text{WE}}$, $\overline{\text{AREADY}}$, $\overline{\text{READY}}$, $\overline{\text{DEN}}$, ALATCH, MEMWIDTH, these indicate that a memory access is in progress, data to memory is on the bus memory is ready next clock cycle, memory is ready this clock cycle, memory read is taking place, memory address on the bus, and an indication of the width of data transfer (word or byte), respectively.

CRU Bus:- Used for serial data transfer, 3 lines provide separate information paths, CRUIN serial input line, CRUOUT serial output line, CRUCLK clock signal gating data.

3 bus arbitration signals $\overline{\text{BUSY}}$, GRANTIN, GRANTOUT. Which indicate requesting device has taken bus, no device with higher priority is requesting the bus, and that a lower priority device may request control of the bus, respectively. GRANTIN and GRANTOUT form a daisy chain priority scheme for transfering bus control. Sync signal, $\overline{\text{BUSCLK}}$ provides synchronisation and must not exceed 10 MHz.

5 Miscellaneous Signals:- $\overline{\text{IORST}}$, $\overline{\text{PRES}}$, $\overline{\text{NMI}}$, $\overline{\text{PWFRFAIL}}$, $\overline{\text{INTEN}}$, which indicate to the system that a system reset is in progress to the I/O devices, power supply has stabilised and processor can begin execution, non maskable interrupt is taking place, a signal from the power supply indicating the loss of primary power, a valid interrupt code is on the bus, respectively.

Analog Signal Bus:- Consists of 3 lines ANAHI, ANALO, ANACOM which can carry analog signal of up to +/− 10V.ANACOM is the ground return path.

Reserved Lines:- Bussed to all slots on the backplane intended for future use.

E-BUS PIN DEFINITION

	ROW A		ROW C	
PIN	SIGNAL	GROUP	SIGNAL	GROUP
1	GND	POWER BUS	GND	POWER BUS
2	$\overline{\text{PRES}}$	CONTROL BUS	$\overline{\text{BUSCLK}}$	CONTROL BUS
3	+12V	POWER BUS	−12V	POWER BUS
4	$\overline{\text{IORST}}$	CONTROL BUS	$\overline{\text{NMI}}$	CONTROL BUS
5	+5V	POWER BUS	+5V	POWER BUS
6	+BATT			
7		RESERVED		RESERVED
8				
9				
10	$\overline{\text{INTEN}}$	CONTROL BUS	ALATCH	CONTROL BUS
11	XA0		XA1	
12	XA2		XA3	
13	A0/D0/INT0		A1/D1/INT1	
14	A2/D2/INT2	ADDRESS/DATA/	A3/D3/INT3	ADDRESS/DATA/
15	A4/D4/INT4	INTERRUPT BUS	A5/D5/INT5	INTERRUPT BUS
16	A6/D6/INT6		A7/D7	
17	A8/D8		A9/D9	
18	A10/D10		A11/D11	
19	A12/D12		A13/D13	
20	A14/D14		A15/D15/CRUOUT	
21	$\overline{\text{AREADY}}$		$\overline{\text{MEMEN}}$	
22	$\overline{\text{DEN}}$		$\overline{\text{READY}}$	
23	$\overline{\text{GRANTIN}}$	CONTROL BUS	$\overline{\text{GRANTOUT}}$	CONTROL BUS
24	$\overline{\text{PWRFAIL}}$		$\overline{\text{BUSY}}$	
25	GND	POWER BUS	GND	POWER BUS
26	+15V		ANAHI	ANALOG BUS
27	ANACOM	ANALOG BUS	ANALO	
28	−15V	POWER BUS	CRUIN	CRU BUS
29	$\overline{\text{WE}}$	CONTROL BUS	+5VSTBY	POWER BUS
30	+5V	POWER BUS	+5V	
31	MEMWIDTH	CONTROL BUS	$\overline{\text{CRUCLK}}$	CRU BUS
32	GND	POWER BUS	GND	POWER BUS

FURTHER INFORMATION:

E-BUS SPECIFICATION
E-BUS DESIGN MANUAL

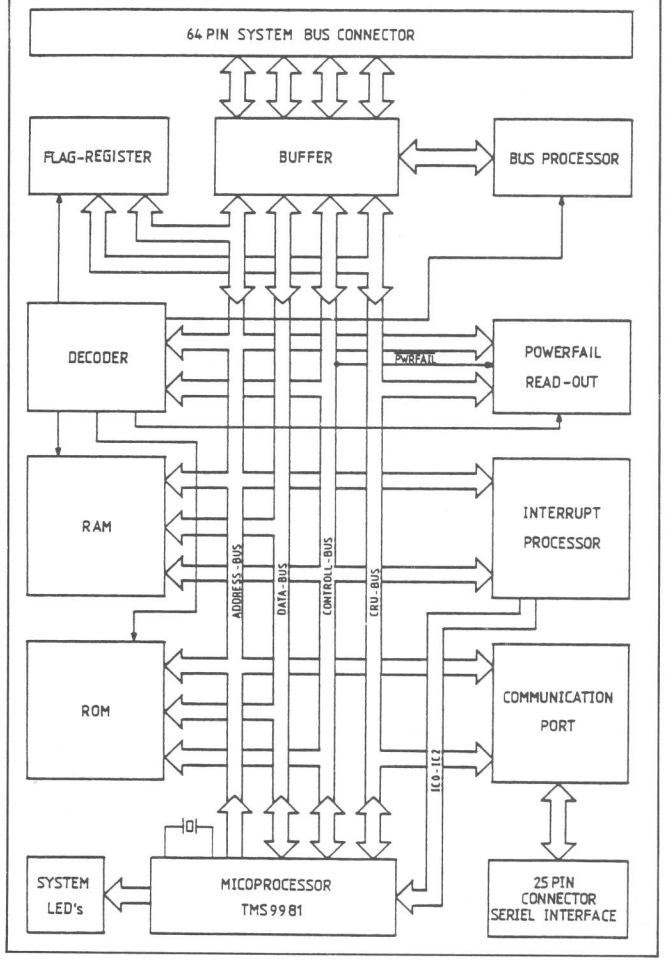
TM990/E150

E-BUS MICROCOMPUTER

FEATURES:

- 16 Bit 9981 Microprocessor.
- Up to 8K bytes EPROM.
- 1K byte on-board RAM.
- 1K bit Flag register.
- 6 Interrupt Levels.
- Serial port EIA/RS232C compatible may be synchronous or asynchronous.
- E-BUS COMPATIBLE, DIN 41612 Connector.
- 0–70°C operating temperature range for HARSH INDUSTRIAL ENVIRONMENTS.
- Factory burnt-in for RELIABILITY.
- COMPACT 100 mm × 160 mm single eurocard.

BLOCK DIAGRAM:



DESCRIPTION:

The TM990/E150 is a Microcomputer (MC) module designed to be the MASTER in a single master E-BUS system.

RAM-Memory
The on board RAM consist of 2X TMS 4045 NL-45 4K static RAM's. It does not require any wait states. The 1K Byte RAM area is located from > 3COO to > 3FFF or > O to > 3FF.

EPROM/ROM Memory
One 28 Pin EPROM/ROM can be used to use TMS 2508, 2516, 2532 and TMS 2564 EPROM's or TMS 4732/4764 ROM. This gives up to 8K Byte on board EPROM. A jumper on the memory decoder selects TMS 2532 or 2564. In the jumper position "TMS 2532" a TMS 2516 or TMS 2508 can be inserted when the loss of 2K or 3K Byte address space can be accepted. If not, a new memory decoder PROM must be generated.

OFF Board RAM/EPROM
The internal RAM/EPROM space can be externally extend to the full 16K Byte address space of the TMS 9981. OFF board ALATCH cycles are generated to accomplish the BUS Spec A0, A1, XA0–XA3 is held low and MEMWIDTH is held high on any external memory cycle.

EIA PORT
The programmable asynchronous/synchronous communication port of the TM990/150 is implemented by the TMS 9902/9903. In addition to the standard RS-232-C interface the μT- and 20 mA TTY-interface is jumper selected. The TM990/150 EIA-Port is identical to P2 of the TM990/100M/101M.

Timer
The TM990/150 has one programmable timer with up to 19.5 ms time interval provided by the TMS 9902 UART.

Interrupt Logic
The TM990/150 supports four external interrupts inputed on the coded INT4 thru INT6 bus lines. INTO–INT3 interrupt lines of the bus are not used.

External and internal $\overline{\text{PRES}}$ and $\overline{\text{NMI}}$ interrupt is also provided. The TMS 9902 interrupt output is connected to the interrupt level 4 of the TMS 9981. The $\overline{\text{PWRFAIL}}$ interrupt of the backplane is set to the level 1 interrupt of the TMS 9981 and can be read out thru the CRU interface.

Flag Register
A 1K bit flag register (TMS 4044 NL-45) is available on the CRU address >800 – FFE and >0 – >3F (WR12), see Appendix B. This can be used in conjunction with the CRU set, reset and test bit instruction for easy control of a large number of flags.

BUS Logic
The E-BUS logic is implemented for single master systems with a DMA mode to allow external (DMA) controller to access the bus. GRANTOUT is directly connected to the GRANTIN with a 2.2KOhm resistor to +5V. All driver and receiver loads to meet the BUS-SPEC.

ORDERING INFORMATION:

TM990/E150-1	MICROCOMPUTER, EPROM SOCKET POPULATED, with TIBUG in TMS 2516. 1K byte RAM, 1K bit FLAGS.
TM990/150-2	OEM VERSION, NO EPROM, NO DOCUMENTATION.

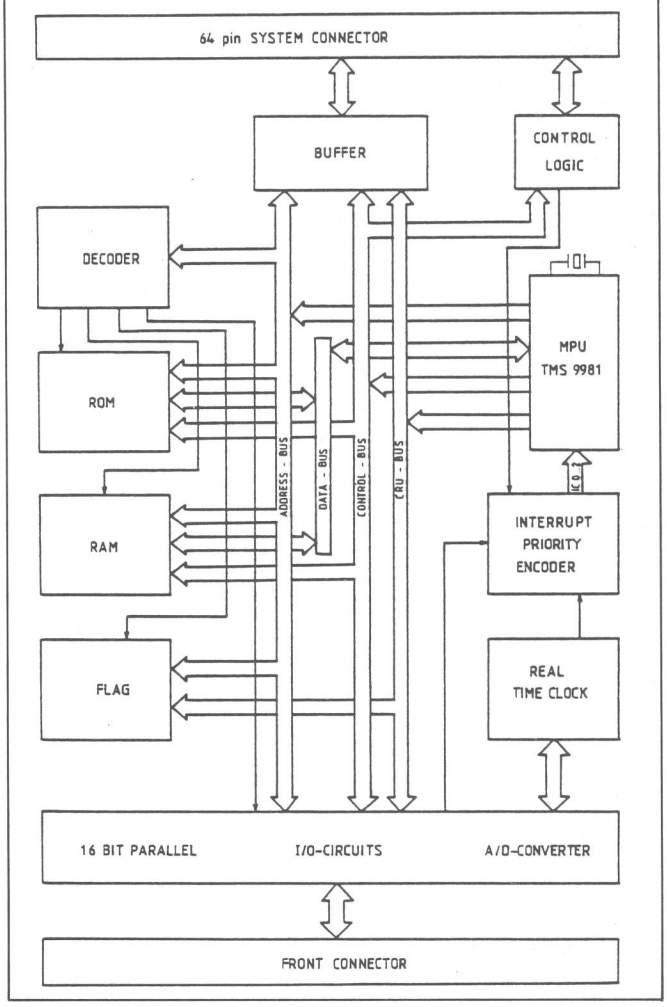
TM990/E151

E-BUS SYSTEM, STANDALONE MICROCOMPUTER

FEATURES:

- 16-bit microprocessor TMS 9981 with on-chip oscillator.
- 1K to 8K byte EPROM's using TMS 2508/16/32/64 or compatible ROM's.
- 2K byte fully static RAM using TMS 2114.
- 1K bit FLAG-register (optional).
- 6 interrupt levels (4 maskable and 2 nonmaskable, RESET and NMI).
- Compatible with the CRU-I/O part of TI's advanced E-BUS system.
- Compatible with standard DIN 41612 connectors, racks and cabinets.
- On board 8 channel A/D-converter with 8 bit resolution (option).
- E-BUS compatible, DIN 41612 connectors.
- 0–70°C operating temperature range for HARSH INDUSTRIAL ENVIRONMENTS.
- Factory burnt in for RELIABILITY.
- COMPACT 100 mm × 160 mm single eurocard.

BLOCK DIAGRAM:



DESCRIPTION:

The TM990/E151 is a single eurocard STANDALONE microcomputer module designed for high volume OEM applications. It has an interface to the E-BUS system for I/O expansion only through the use of TI's CRU Command Driven I/O architecture.

MICROPROCESSOR UNIT (TMS 9981 MPU)
The TMS 9981/TMS 9981 NL microprocessor is used as the Micro-Processor Unit at 10 MHz clock rate. This gives a 2.5 MHz system clock frequency.

CONTROL LOGIC
The control-logic generates a reset signal during power on sequence and also if PRES- (power reset) is active. Also it generates an IORSET-signal for all I/O-circuits.

An on board reset switch is not provided. This function might be implemented externally by pulling the PRES- line low.

ON BOARD MEMORY
The on board memory area provides for enough ROM and RAM to cover the applications foreseen for the board.

RAM MEMORY
The on board RAM-area consists of 4 × TMS 4045 4K static RAM's which do not require any wait states. The 2K byte RAM area is located from >3800 to >3FFF (see also Appendix A).

ROM MEMORY
One 28 pin socket can be used for ROM's or EPROM's with a single +5V supply voltage. These are EPROM's of the series TMS 25XX (TMS 2508/16/32/64) and ROM's of the TMS 47XX series. These give up to 8K byte program area to the user. The ROM memory area is located in the lower memory area from >0 to >1FFF.

FLAG REGISTER
A 1K bit FLAG register (TMS 4044) is available at the CRU address >800 to >FFE (WR 12, see also Appendix B). This can be used in conjunction with all CRU instruction to easily control of a large number of flags.

INTERRUPT LOGIC
The TM990/TM990/E151 supports four maskable static interrupts and two nonmaskable. These are:

- RESET (non maskable)
- NMI (non maskable)
- POWER FAIL (level 1)
- ADC (level 2)
- CLOCK (level 3)
- INTEN (level 4)

All interrupts are changed into a code, by the interrupt priority encoder (ICO..2) for the TMS 9981.

BUS BUFFER
The bus interface is a reduced E-BUS interface, it allows only CRU-Expansion. Therefore the following signals are necessary:

- Address Lines A0 to A14
- CRUCLK-
- CRUOUT
- BUSCLK
- IORSET
- BUSY (always LOW)
- MEMEN-

The bus drivers can be disabled (jumper selectable). Therefore, it is possible to plug this microcomputer board into a TM990/E-Microcomputer system as a stand alone computer.

TTL I/O CIRCUITS
The I/O area consists of 16 TTL inputs (2 ×SN74LS251) and 16 TTL outputs (2 × SN74LS259). The ports can be easily controlled via CRU.

Three output ports and one input port are needed for the TI-BUS interface, if an IIL-Clock is used. An additional input port is needed for the POWERFAIL-Identification, if a POWERFAIL/Routine is used (jumper selectable).

A/D-CONVERTER
The used ADC 0808 is a new TI device in CMOS technology.

- 8 Bit Resolution
- Total Unadjusted Error ×/– 1/2 LSB
- 100 µs Conversion Time
- Latched 3-state Outputs
- Single 5-Volt Supply

After each conversion the device generates an interrupt (level 2) to indicate the end of conversion.

ORDERING INFORMATION:

TM990/E151-2 1K Byte RAM, socket for further 1K byte. No a/d, clock or flag register.

TM990/E151-3 TM990/E151-1 with no RTC clock chip.

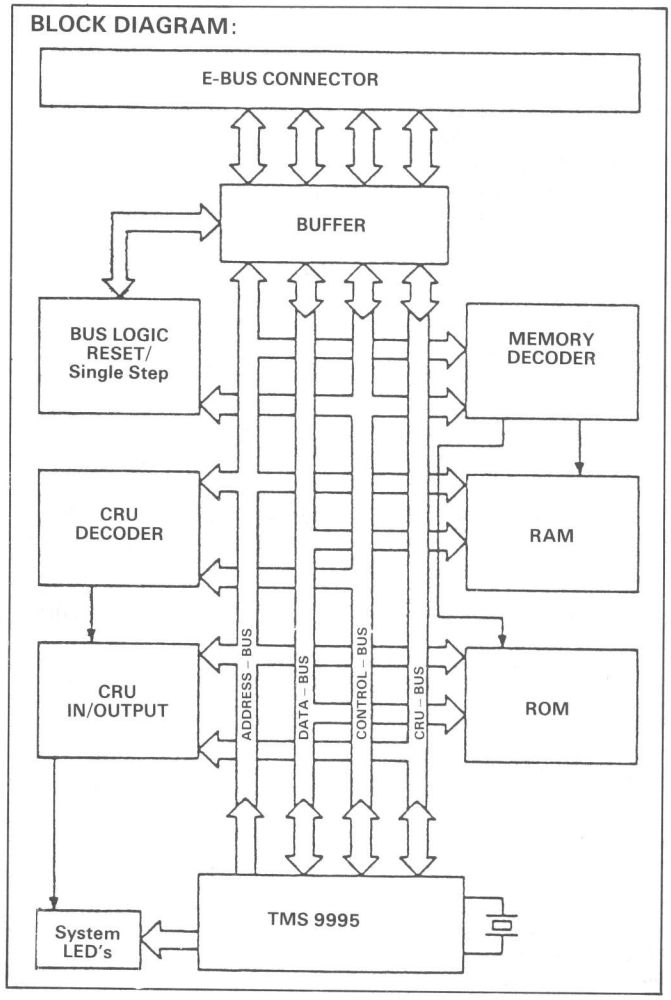
TM990/E155

E-BUS MICROCOMPUTER

FEATURES:

- 12 MHz, 16 Bit 9995 microprocessor.
- 64K byte physical address space.
- 1M byte logical address space using CRU BANK SWITCHING.
- Up to 16K byte EPROM.
- Up to 4K byte static RAM.
- 6 interrupt levels.
- On board TIMER/EVENT COUNTER.
- On board 16 Bit FLAG REGISTER.
- E-BUS compatible, DIN 41612 Connector.
- 0–70°C operating temperature range, for harsh industrial environments.
- Factory burnt in for RELIABILITY.
- COMPACT 100 mm × 160 mm single eurocard.
- Single 5V supply.

BLOCK DIAGRAM:



DESCRIPTION:

The TM990/E155 is a microcomputer (MC) module deisgned to be a MASTER in a single master E-BUS system. It uses TI's 9995 microprocessor, which features on-chip RAM, TIMER & FLAG REGISTER, and using a 12 MHz crystal clock benchmarks at between 1.5 and 3.0 times the throughput of a 3 MHz TMS 9900. A 16 Bit by 16 Bit multiply instruction takes just 7.67 μS to execute. The TM990/E155, uses TI's unique Command Driven I/O architecture (CRU) to access the four most significant address lines of the E-BUS backplane (XA0–XA3) to effectively expand the address capability of the 9995 from 64K bytes to 1M byte, through a "bank switching" mapping technique.

CONTROL LOGIC

The control logic generates a reset signal during the power-on sequence. A PRES- signal, fed from the system bus to this circuitry, forces a CPU reset as well as generating the IORST-signal. All CRU-modules attached to this signal on the system bus will thereby be set to a proper condition during power up.
The TM990/E155 control logic also contains single-step logic which allows the execution of a single instruction under software control.
The LREX instruction generates the LREX-Pulse (external instruction) which activates the Single-Step Logic, ending in an NMI interrupt on completion of the single instruction execution.
The NMI-Interrupt from the E-Bus goes directly to the MPU and therefore the NMI can also be used as a normal Interrupt.

On Board Memory

On the TM990/E155 there are three ways to change The Memory Map. A jumper is installed for selecting the ROM (32K/64K) size. The other two signals are changeable via CRU (see section 3.5). These are RAM HIGH/LOW and Memory Map 0/1. Since in memory map 1 the on-board memory can be disabled, the names of the signals RAM L/H and ROM 32/64 only make sense in the Memory Map 0. In Memory Map 1 the user can employ these signals to select one of the four other different Memory maps.

Memory Map Applications

This feature, plus the separate on-board areas allows the use of different standard Software Systems in one Hardware configuration. A small program in the on-chip RAM area can control this switching by CRU. E.g. use EUROBUG 4 for program debugging, and in the same system, have the possibility to switch to POWER BASIC which is installed at the Memory address >0000 on a Memory expansion board. If the user switches off the on board Memory and goes with a BLWP to address >0000 he is automatically in POWER BASIC. For this he has two possibilities, to switch off the whole on-board Memory, if he has a RAM expansion on address >F000 to >FFFF, or only on-board ROM. If bank switching is used, 17 different programs can be chosen in this way.

RAM Memory

The on-board RAM area consists of two TMS 4016 devices. Each of those devices is organised as 2K × 8-Bits. RAM's used must have an access time without wait states of less than 130 ns, and with one wait, less than 460 ns. The two chips are wired to provide 4K-bytes of RAM.

ROM Memory

Two 28 pin sockets may be used for several different ROM/EPROM devices with a single +5V supply voltage. These are EPROM's of the TMS 25XX series. It is also possible to use pin-compatible ROM's (e.g. TMS 4732).
The EPROM's or ROM's used must have an access time without wait states of less than 95 ns, and with one wait state, less than 428 ns.
The standard memory map is set up for TMS 2532 and TMS 2564 EPROM's (jumper selectable).

On-board CRU

ADDR. WR 12	CRU ADDR.	CRU READ	CRU WRITE
–0000–	–0000–		
–013E–	–009F–		
–0140–	–00A0–	PWRF–IDENTIFICATION	ERROR LED
–0142–	–00A1–	INT4–IDENTIFICATION	NOT USED
–0144–	–00A2–	RAM HIGH/LOW	RAM HIGH/LOW
–0146–	–00A3–	MEMORY MAP0/1	MEMORY MAP 0/1
–0148–	–00A4–	XA3	XA3
–014A–	–00A5–	XA2	XA2
–014C–	–00A6–	XA1	XA1
–014E–	–00A7–	XA0	XA0
–0150–	–00A8–	SAME BLOCK REPEATED	
–015E–	–00AE–		
–FFFE	–7FFF–		

On-Board CRU Map

There are 8 CRU in- and output bits used on the CPU board. For these bits, the addresses are not fully decoded, therefore they all have two different addresses (e.g. bit 0: >140 and >150 in WR12). After a RESET, all output bits are LOW.

ORDERING INFORMATION:

TM990/E155-1 EPROM sockets unpopulated.
TM990/E155-2 RAM & EPROM sockets unpopulated.

POWER-FAIL Identification

At this CRU address the status of the POWER FAIL-interrupt line from the back-panel can be read. This feature is useful after executing a power fail routine. After all vital data has been saved, the routine can test the POWER FAIL line and decide whether to go into the IDLE state (interrupt still active), or to resume normal operation (interrupt no longer present, was probably caused by a short power glitch).

INT4-Identification

The TM990/E155 uses the INTEN- line as a static common interrupt line, connected to the INT4 input of the TMS 9995 CPU. Therefore the INT4-identification, at >142 in WR12, can be used to test the INTEN-line. A signal on INT4 means that some interrupt was received from the bus, and polling must be used to determine which one. At the end of an INT4 activated routine, after the source of the interrupt has been cleared, if the INT4-identification line is still low (active), another interrupt has occurred in the meantime and is pending, and the processor may avoid some delay in processing the new interrupt by immediately resuming the polling process.

ERROR LED

The output bit (>140) is connected to the error LED, and can be switched on and off. Please note, that the LED is initially ON after reset. It is off when the CRU bit is one.

Extended Address Lines (XA0–XA3)

The TM990/E155 has a directly addressable memory area of 64K byte. Via CRU it is possible to control the Extended Address lines (XA0–XA3). This allows bank switching and gives access to a memory area of up to 1M Byte (16 banks with up to 64K bytes each).

Interrupts

Four of the 6 Interrupts of the TMS 9995 are at the user's disposal. Four Interrupts are maskable, PRES- and NMI- are non-maskable. Table 1 shows the interrupt assignment.

Table 1: Interrupt Data

Use	Interrupt level	Function	
PRES-	0	RESET	Highest priority
NMI-	—	Non-Maskable-Interrupt (LOAD, single step)	
INT1	1	POWERFAIL	
INT2	2	Arithmetic overflow, MID	
INT3	3	Internal Decrementer	
INT4	4	INTEN-*	Lowest priority

*This Interrupt line is used as static common interrupt line.

SYSTEM LED's

There are three LED's on the front edge of the board.
The upper one is the red IDLE LED. This LED is controlled by the IDLE pulse, and it is ON if the processor is in the IDLE state.
The second one is the green RUN LED. It is controlled by the IAQ pulse of the processor. If the processor is executing instructions, this LED will be ON.
The last one, is a red ERROR LED. It is controlled via CRU (see section 3.5.1), and is initially ON after reset. It should then normally be extinguished by the user software after a successful self-test.

TM990/E250

E-BUS MEMORY AND I/O EXPANSION MODULE

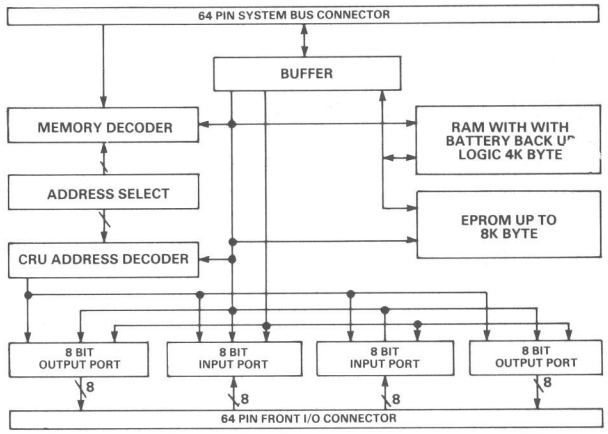
FEATURES:

- **Up to 4K bytes of static RAM.**
- **BATTERY BACKUP Option for RAM.**
- **Up to 8K bytes of EPROM.**
- **16 TTL compatible inputs.**
- **16 TTL compatible outputs.**
- **E-BUS COMPATIBLE, DIN 41612 Connector.**
- **DIN 41612 Standard I/O Connector.**
- **0–70°C Operating Temperature range for HARSH INDUSTRIAL ENVIRONMENTS.**
- **Factory Burnt in for RELIABILITY.**
- **COMPACT 100 mm × 160 mm Single eurocard.**
- **Single 5V supply rail.**

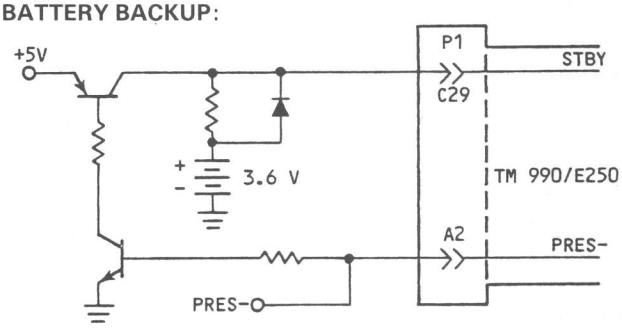
DESCRIPTION:

The TM990/E250 is a combination memory and I/O expansion (MIE) module designed to work with TI's popular range of E-BUS eurocard standard MICROCOMPUTERS. Both the RAM and EPROM memory blocks can be mapped into E-BUS SYSTEM memory, using Dual-In-Line (DIL) switches on board. Designed for REALTIME Systems, the memory control circuits make use of the standard E-BUS signal PRES- to limit access to the RAM during power-up, power-down and 'brown-out' sequences. Additionally a facility for using the E-BUS Standby option, to provide for non-volatile data or program storage in the absence of primary power. The I/O is accomplished using TI's unique Command Driven I/O architecture, the Communications Register Unit ('CRU') allowing direct access to single or multiple bits of either input or output using single instructions. The TM990/E250 provides DIL switches for the selection of the CRU base address.
The I/O is configured as four ports of 8-bits each, the two output ports using SN74LS259 latches; the inputs using SN74LS251 circuits. Both these IC's utilise Robust Schottky Bipolar technology for excellent drive capability. A self-test facility could be provided by the user by looping back an output port to an input port off board. Both the E-BUS and I/O connectors conform to DIN 41612 standards for reliability and a wide range of compatible racking equipment is available for the standard 100 mm × 160 mm Single Eurocard.

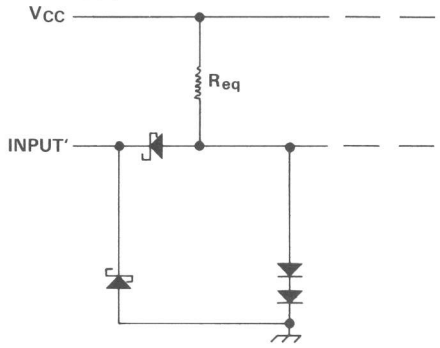
BLOCK DIAGRAM:



BATTERY BACKUP:

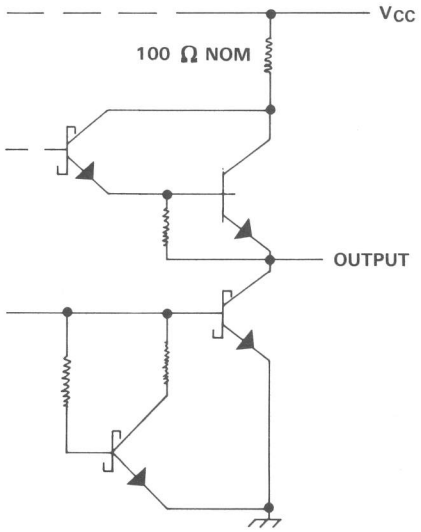


TYPICAL INPUT:



A, B, C, S: R_{eq} = 20 k Ω NOM
D0 thru D7: R_{eq} = 17 K Ω NOM

TYPICAL OUTPUT:



ORDERING INFORMATION:

TM990/E250-1	FULLY POPULATED 4K bytes RAM & I/O, NO EPROM.
TM990/E250-2	2Kbytes RAM, NO I/O OR CONNECTOR.

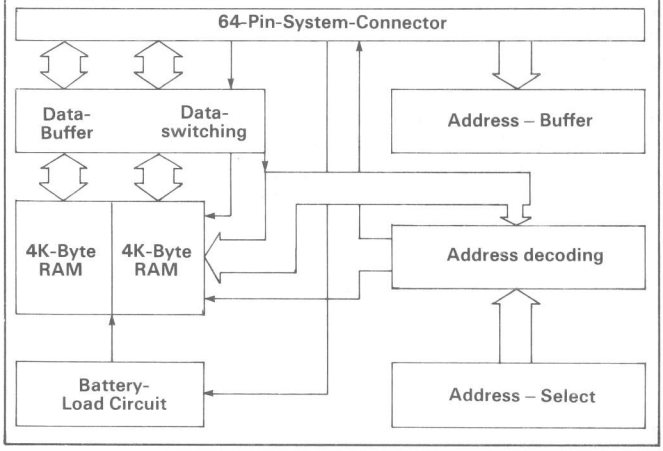
TM990/E251

E-BUS RAM MEMORY EXPANSION MODULE

FEATURES:

- Up to 8K bytes of Static RAM.
- Compatible with NMOS or CMOS RAMS.
- BATTERY BACKUP option, on or off board.
- MINIMUM 350 HOURS data retention with CMOS RAMS and on board 70 mAH Battery.
- 8 or 16 bit Data width.
- Selectable number of Wait States.
- Mappable anywhere in E-BUS 1Mbyte SYSTEM RAM.
- E-BUS COMPATIBLE, DIN 41612 Connector.
- 0–70°C temperature range, for HARSH INDUSTRIAL ENVIRONMENTS.
- 100 mm × 160 mm COMPACT single eurocard format.
- Factory Burnt in for RELIABILITY.

BLOCK DIAGRAM:



DESCRIPTION:

The TM990/251 is a RAM memory expansion memory (RME) module designed to work with TI's popular range of E-BUS eurocard standard MICROCOMPUTERS. The E-BUS system 20 bit address range is fully decoded on board by means of Dual-In-Line (DIL) switches, giving a start address alterable in 2Kbyte steps. Standalone system operation is facilitated by the use of the E-BUS PRES- signal to protect on board data during power-up, power-down and 'brown-out' sequences. Two different mechanisms to provide non-volatile data storage are provided; the first uses the +5 VSTBY supply rails provided by the E-BUS backplane (the user must ensure his power supply will provide this standby supply during primary supply failure). Alternatively the user may use plug compatible CMOS RAMS, in which case the optional on board battery will provide backup. The selection between +5 VSTBY and on board battery is made via jumpers. The E-BUS connector conforms to DIN 41612 standards for reliability, and a wide range of compatible racking equipment is available for this standard 100 mm × 160 mm single eurocard.

WAIT STATE TABLE:

max. access time from address	max. access time from Chip select	required wait states TM990/E150, 2,5 MHz BUSCLK
440 ns	255 ns	0
840 ns	655 ns	1
1240 ns	1055 ns	2
		TM990/E155 3 MHz BUSCLK-
—	—	0
415 ns	310 ns	1
750 ns	640 ns	2

Required wait states

POWER CONSUMPTION:

Battery: 3,6V NiCd Battery 70 mAH

Power Supply:	+5V type	+5V max	+5V typ	STBY* max
without RAM	700 mA	1100 mA		
with RAM	960 mA	1400 mA	260 mA	360 mA

*TM990/E251-1

ORDERING INFORMATION

TM990/E251-1 FULLY POPULATED 8Kbyte NMOS RME MODULE, NO BATTERY OR LOAD CIRCUIT.

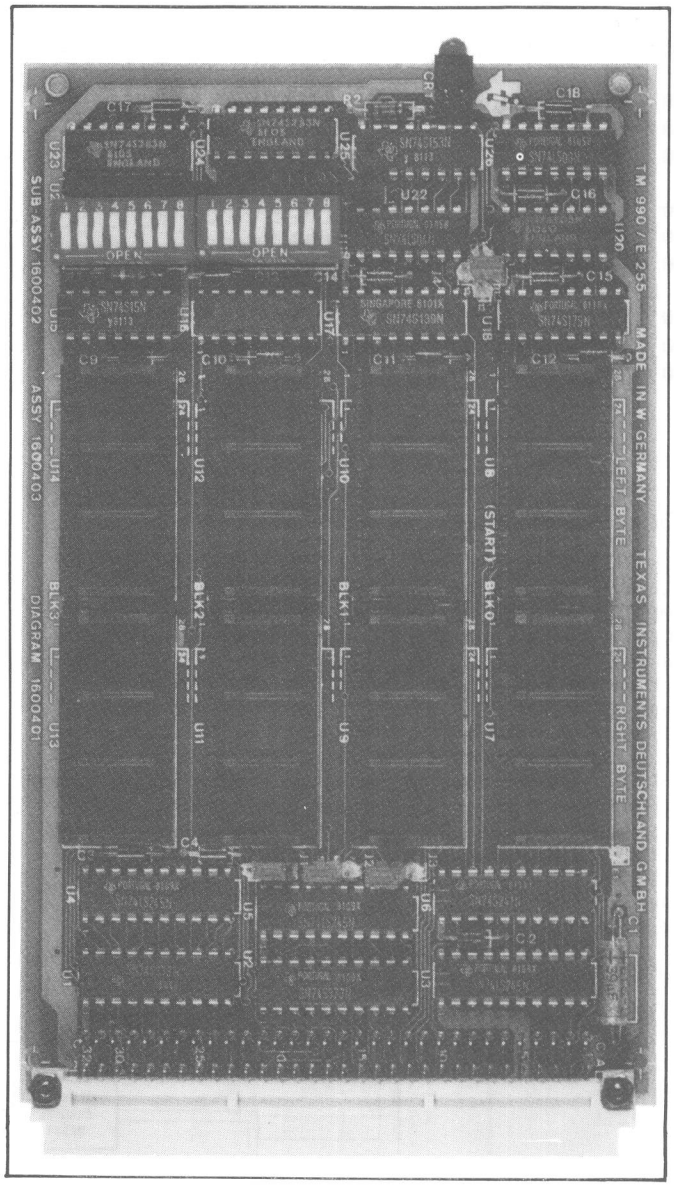
TM990/E251-2 BATTERY AND LOAD CIRCUIT INCLUDED, SOCKETS ONLY FOR UP TO 4 RAM DEVICES.

TM990/E255

EBUS EPROM MEMORY EXPANSION MODULE

FEATURES:

- Up to 64K bytes of EPROM.
- 8 or 16 bit data.
- E-BUS COMPATABLE, DIN 41612 Connector.
- 0–70°C FOR HARSH INDUSTRIAL ENVIRONMENTS.
- 100 mm × 160 mm COMPACT single eurocard.
- Factory burn in for RELIABILITY.
- 20 bit address bus decoding.



Power Supply (typ): ..... + 5V @ 750 mA
— w/o EPROM.

ORDERING INFORMATION:

TM990/E255 SHIPPED WITHOUT EPROM. SOCKETS FOR TMS2516, 2532, 2564 SUPPLIED.

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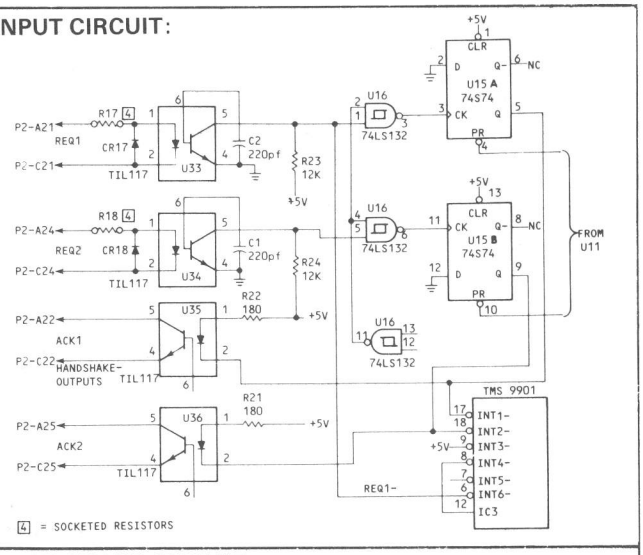
TM990/E350

E-BUS INPUT EXPANSION MODULE

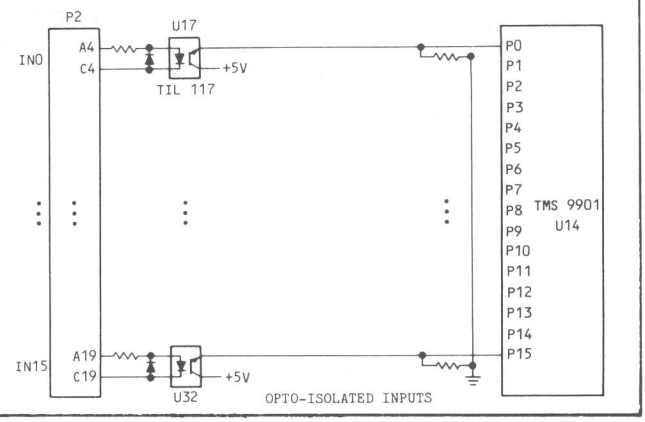
FEATURES:

- **16 opto-isolated inputs, with up to 250V common mode rejection.**
- **2 opto-isolated "handshake" channels.**
- **2 positive EDGE TRIGGERED INTERRUPTS.**
- **PROGRAMMABLE TIMER with up to 420 mS time intervals.**
- **E-BUS COMPATIBLE, DIN 41612 Connector.**
- **DIN 41612 standard I/O Connector.**
- **0–70°C operating temperature range for HARSH INDUSTRIAL ENVIRONMENTS.**
- **Factory burnt in for RELIABILITY.**
- **COMPACT 100 mm × 160 mm single eurocard.**
- **Single 5V supply.**

INPUT CIRCUIT:



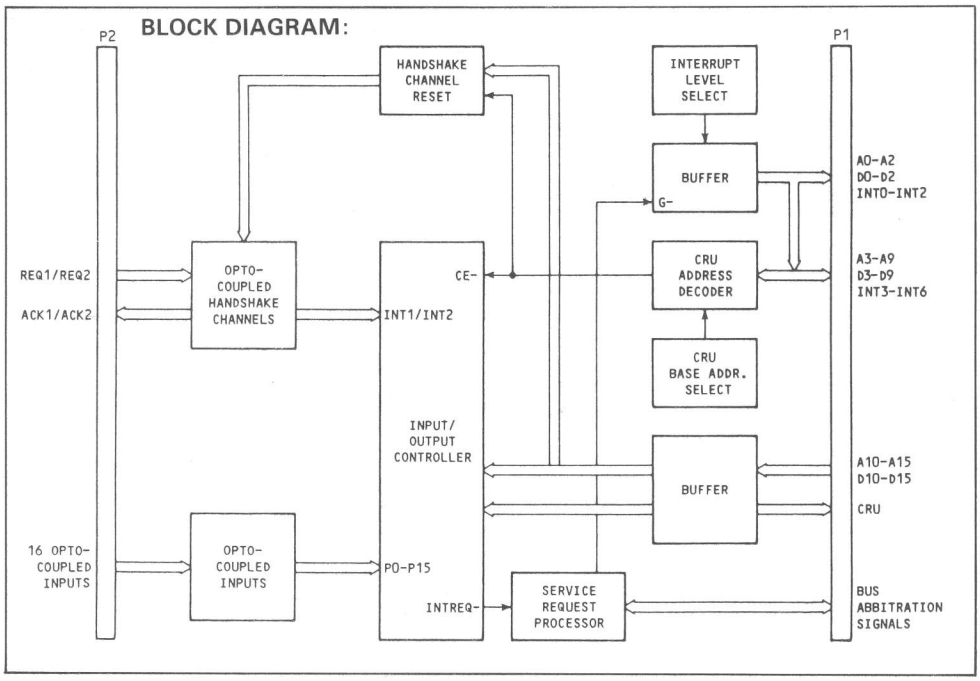
HANDSHAKE CIRCUIT:



DESCRIPTION:

The TM990/350 is an Input Expansion (IE) module designed to work with TI's popular range of E-BUS eurocard standard MICROCOMPUTERS. The 16 input lines are isolated inputs using TIL117 opto-couplers. Either TTL compatible inputs are available as standard or the user may select the version without series resistors factory fitted for almost any required input voltage. The I/O is implemented using TI's unique Command Driven I/O architecture, the Communications Register Unit (CRU), allowing direct access to single or multiple bit inputs without resorting to time-consuming software masking routines or using the E-BUS memory space. The CRU is used to interface with an on board TMS 9901 Programmable System Interface IC, and allows the inputs to be mapped any where in 4Kbit CRU address space through the use of Dual-In-Line (DIP) switches. Additionally the E-BUS SYSTEM interrupt scheme is implemented allowing the interrupts generated to be routed to any one of 8 E-BUS Multi-microcomputers.

BLOCK DIAGRAM:



ORDERING INFORMATION:

TM990/E350-1	FULLY POPULATED, TTL INPUT LEVELS.
TM990/E350-2	NON-TTL INPUT OPTION, NO SERIES LIMITING INPUT RESISTORS SUPPLIED.

TM990/E351

E-BUS OUTPUT EXPANSION MODULE

FEATURES:

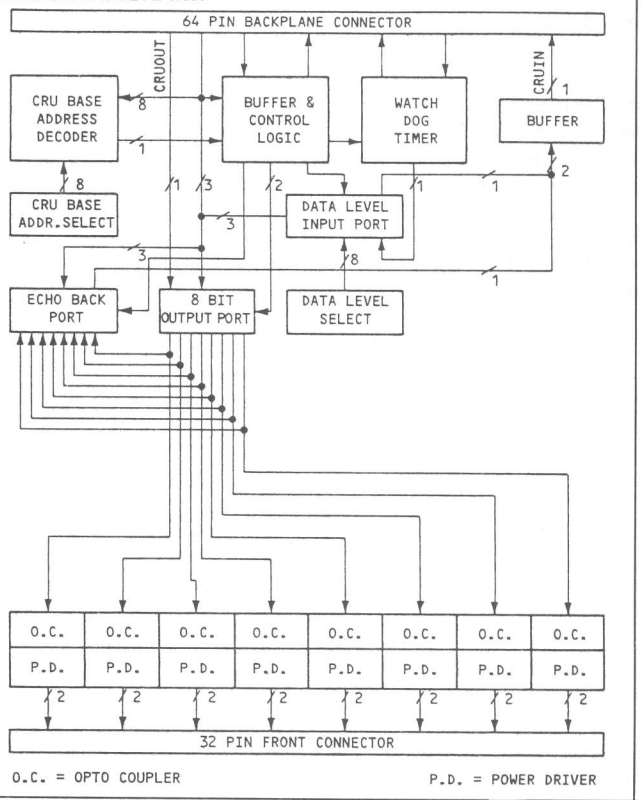
- **8 opto-isolated power outputs.**
- **1.2 Amp drive capability each.**
- **On board dual WATCHDOG TIMER.**
- **Echoback logic for SELTESTING.**
- **8-bit constant input DIP switch.**
- **E-BUS COMPATIBLE, DIN 41612 connector.**
- **DIN 41612 I/O connector (P2).**
- **0–70°C operating temperature range for HARSH INDUSTRIAL ENVIRONMENTS.**
- **Factory BURNT IN, for REALIABILITY.**
- **COMPACT 100 mm × 160 mm single eurocard.**
- **Single 5V supply rail.**

DESCRIPTION:

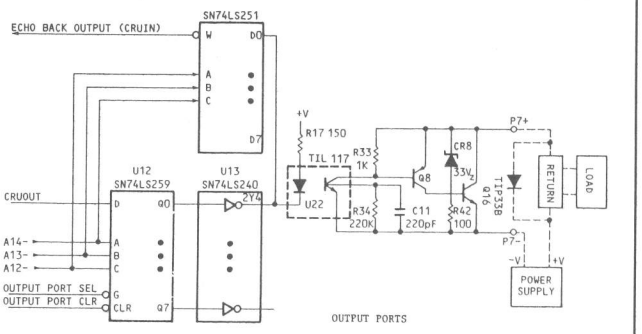
The TM990/E351 is an Output Expansion (OE) module designed to work with TI's popular range of E-BUS standard MICROPROCESSORS. The eight output lines are all opto-isolated, giving 500V isolation between two channels or ground, feature a 1.2 Amp DC sink capability using rugged TIP33 power transistors. Withstanding voltages of up to 30, these outputs are ideal for direct drive of relays, lamps, or motors in 5 to 24V systems. The outputs are implemented using TI's unique command driven I/O architecture, the Communications Register Unit (CRU), allowing direct access, in a single instruction, to single or multiple bits of output, without resorting to time consuming software masking routines.

The on board WATCHDOG TIMER provides the user with a powerful tool to identify corrupt program sequences and thus protect the system interfaces and attached peripherals from malfunction. The TM990/E351 has two timeouts, the first is started after reset, giving a 20 mS period after which a PWRFAIL- or LOAD- interrupt (jumper selectable) is generated so the system is given the chance to re-initialise. Whether the outputs are reset at this stage is jumper selectable. The second timeout, of 10 mS, starts after the first, and if not reset will cause a system HOLD by asserting GRANTOUT (jumper selectable). Once in HOLD the system can only be restarted with a SYSTEM-RESET.

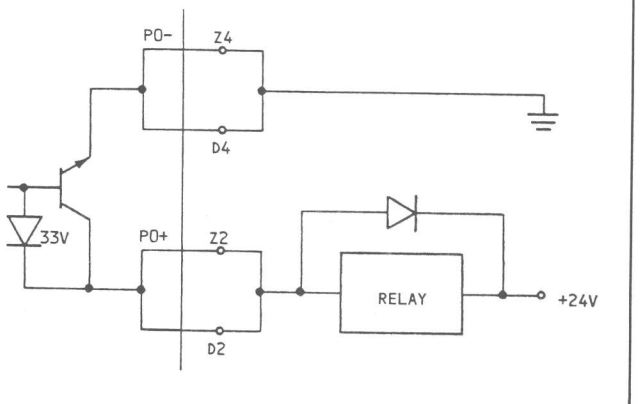
BLOCK DIAGRAM:



OUTPUT DRIVER CIRCUIT:



DRIVING A 24V RELAY:



ORDERING INFORMATION:

TM990/E351-1 Fully populated with DIP constant switch and timer and manuals.

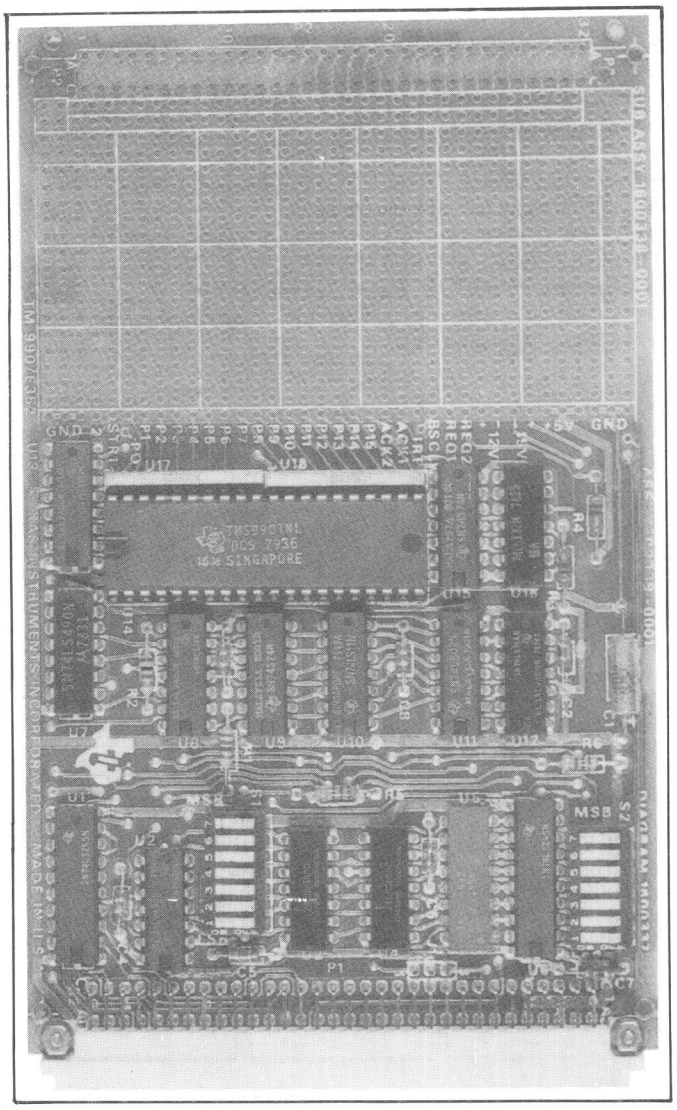
TM990/E351-2 OEM version, no manuals, DIP switch or timer.

TM990/E352

E BUS UNIVERSAL I/O MODULE

FEATURES:

- 16 TTL Compatible I/O lines.
- 2 'HANDSHAKE' lines.
- 37 × 19 hole PHOTOTYPING AREA.
- PROGRAMMABLE TIMER with up to 420 mS interval.
- EBUS COMPATIBLE, DIN 41612 Connector.
- 0–70°C Operating temperature and 0–95%. Humidity (non-condensing) FOR HARSH INDUSTRIAL ENVIRONMENTS.
- Factory burnt in for RELIABILITY.
- COMPACT 100 mm × 160 mm single eurocard.
- Single 5V supply.



Power Supply (typ): ..... 5V @ 600 mA

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ORDERING INFORMATION

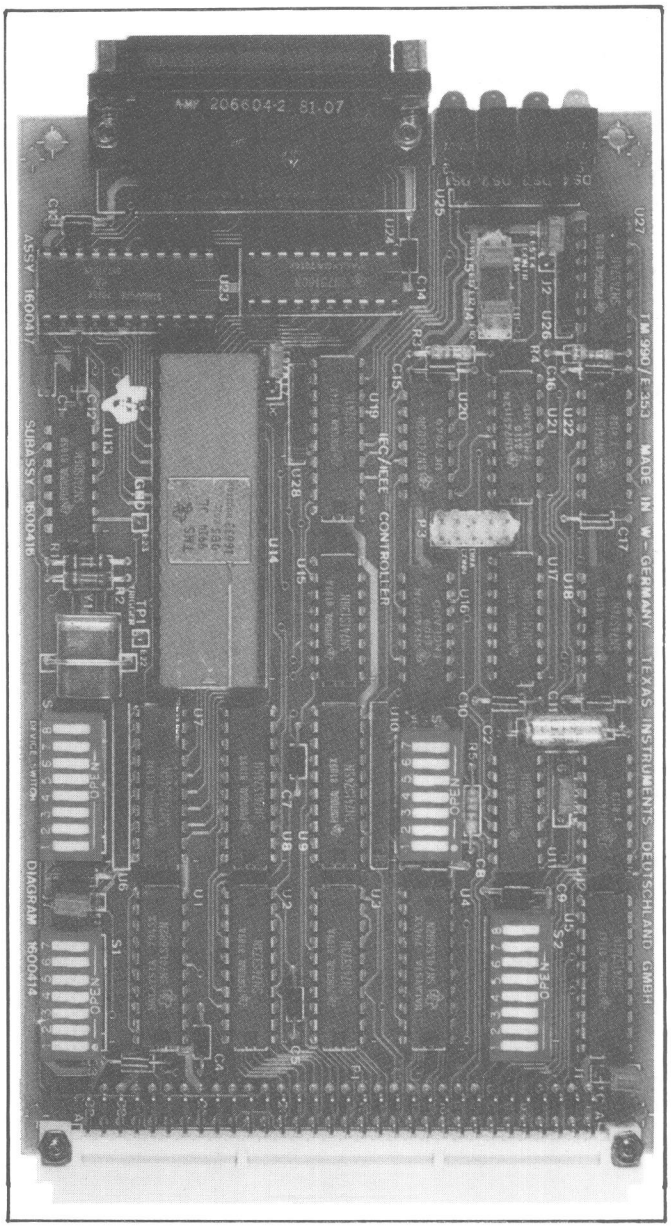
TM990/E352 UNIVERSAL INPUT/OUTPUT MODULE

TM990/E353

IEEE 488 ('GPIB') BUS INTERFACE

FEATURES:

- Conforms to 1975/78 IEEE 488 SPECIFICATION.
- LISTENER, TALKER AND CONTROLLER FUNCTIONS.
- Automatic Send/Receive handshake.
- Interface for DMA operation.
- Status LED's for REN, SRG, DAV, CONTROL.
- IEC 6622 connector to IEEE BUS.
- Up to 250 KBS OPERATION.
- Memory MAPPED.
- EBUS Computable, DIN 41612 connector.
- 0–70°C operating temperature range, FOR HARSH INDUSTRIAL ENVIRONMENTS.
- Factory burnt in for RELIABILITY.
- Compact 100 mm × 160 mm single eurocard.
- Single 5V supply rail.



Power Supply: (typ) .....5V @ 750 mA

ORDERING INFORMATION:

TM990/E353 GPIB BUS INTERFACE MODULE.

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E-BUS ACCESSORIES

Boards

TM990/E5000
Rear panel board for 19" housing with 12 plug positions; connections for power supply and several control lines, with watchdog timer. Plug type: DIN 41612.

TM990/E5011
Extender Board. Makes it possible to operate boards outside the chassis for testing and checking purposes.

TM990/E5013
Prototype board for wire-wrap circuits. Prefabricated board in European format with E-BUS-connection for user-specific circuitry.

Power Packs

TM990/518
OEM power pack (open chassis) +5V/6.0A, +12V/0.9A, −12V/0.9A, −45V/0.1A. Overvoltage protection at +5V, current limiter for +5V and +12V.

TM990/518A
Power Pack (cased) +5V/4.0A, +12V/0.6A, −12V/0.4A, +45V/0.1A, otherwise like TM990/518.

TM990/519
Power Pack (cased), +5V/2A, +12V/0.35A, −12V/0.2A.

Accessories: Cable

TM990/502
I/O connector cable.

TM990/503
I/O connector cable for 743 KSR/745 terminals.

TM990/504
Connector cable.

TM990/505
I/O connector cable for 733 ASR.

OTHER:
TM990/E50004 – 4 slot (3V) chassis.